US009209815B1

(12) **United States Patent**
Taylor

(10) **Patent No.: US 9,209,815 B1**
(45) **Date of Patent: Dec. 8, 2015**

(54) **THYRISTOR-BASED OPTICAL CHARGE PUMP FOR AN OPTICAL PHASE LOCK LOOP**

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(72) Inventor: **Geoff W. Taylor**, Mansfield, CT (US)

(73) Assignees: **Opel Solar, Inc.**, Storrs Mansfield, CT (US); **The University of Connecticut**, Farmington, CT (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/579,151**

(22) Filed: **Dec. 22, 2014**

(51) **Int. Cl.**
H03L 7/06 (2006.01)

(52) **U.S. Cl.**
CPC ***H03L 7/06*** (2013.01)

(58) **Field of Classification Search**
USPC 327/147–149, 156–158
See application file for complete search history.

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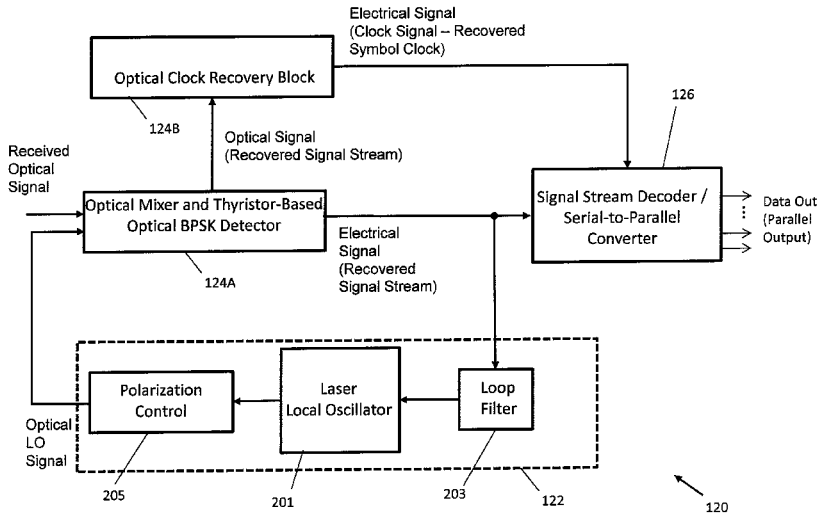
Primary Examiner — Adam Houston
(74) *Attorney, Agent, or Firm* — Gordon & Jacobson, P.C.

(57) **ABSTRACT**

A charge pump circuit for an optical phase lock loop, which includes first and second optical thyristors configured to receive respective first and second digital optical signal inputs. A first control circuit receives a first digital electrical signal input corresponding to the second digital optical signal input, and a second control circuit receives a second digital electrical signal input corresponding to the first digital optical signal input. The first control circuitry controls switching operation of the first optical thyristor that sources current to a first filter circuit in response to the levels of the first digital optical signal input and the first digital electrical signal input. The second control circuitry control switching operation of the second optical thyristor that sinks current from a second filter circuit in response to the levels of the second digital optical signal input and the second digital electrical signal input.

21 Claims, 43 Drawing Sheets



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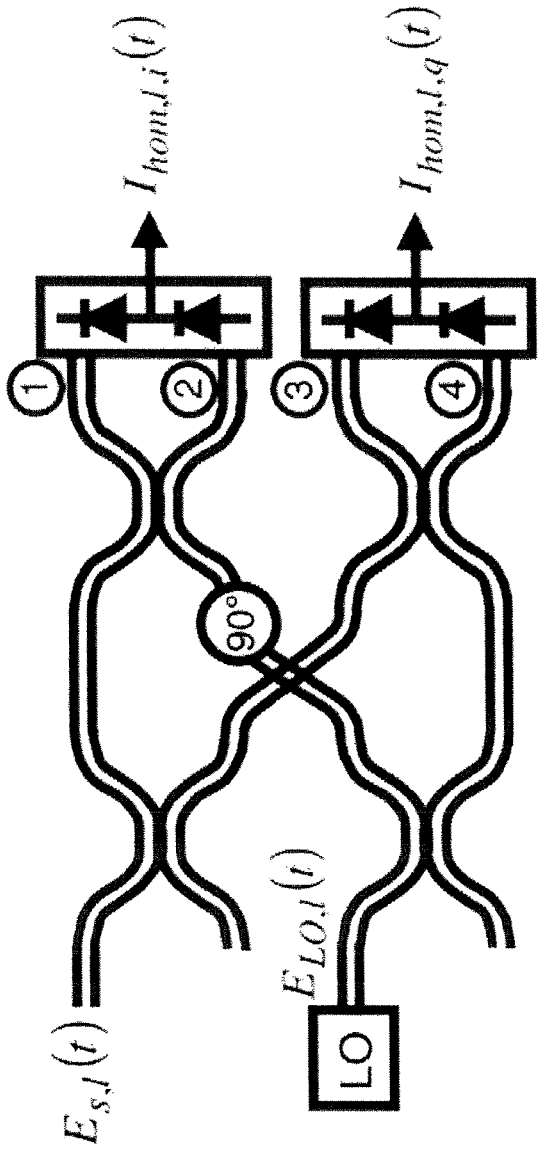


PRIOR ART

FIG. 1

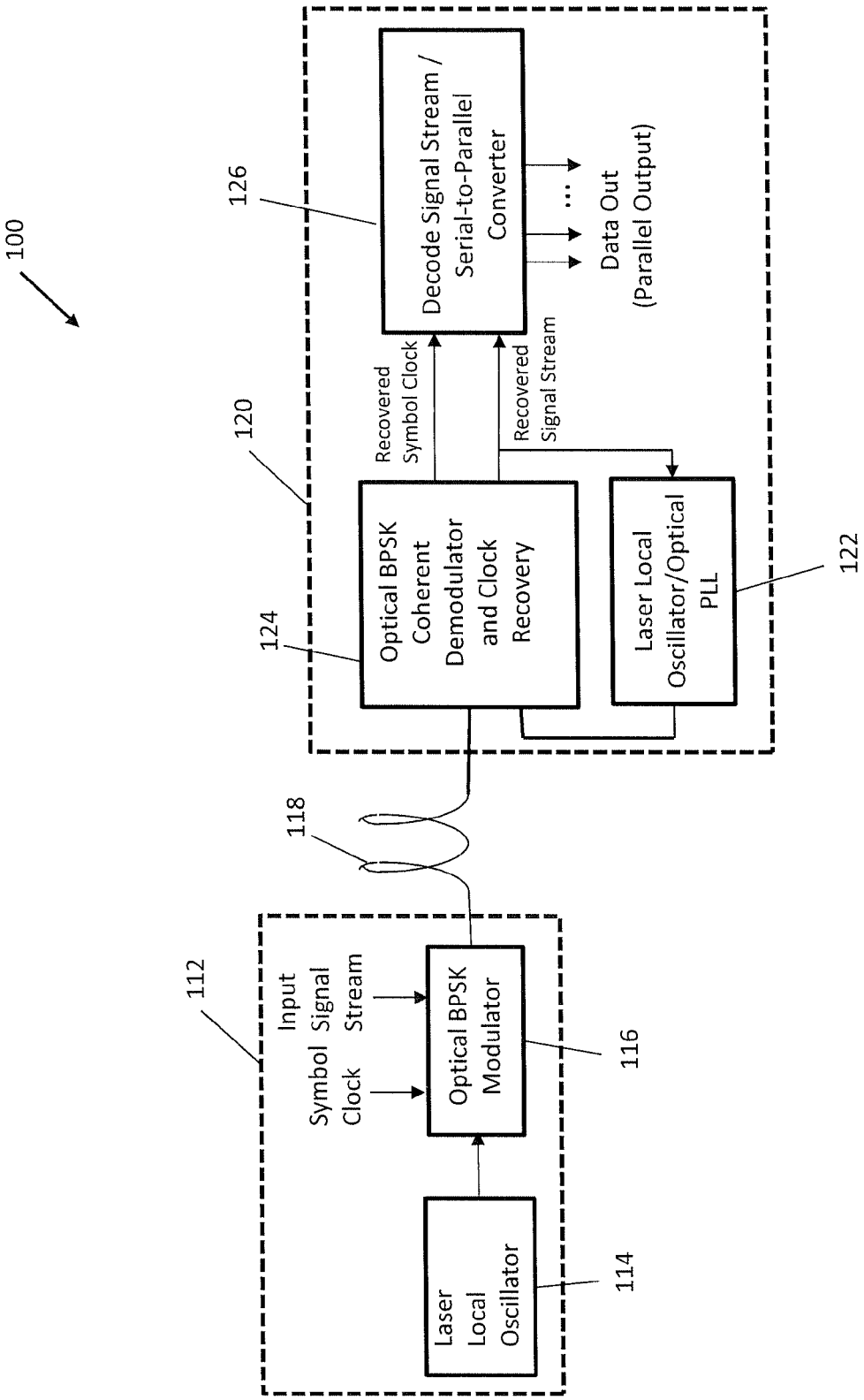

100
112
Input Symbol Clock
Signal Stream
Optical BPSK Modulator
116
Laser Local Oscillator
114
118
120
Recovered Symbol Clock
Recovered Signal Stream
Optical BPSK Coherent Demodulator and Clock Recovery
124
Laser Local Oscillator/Optical PLL
122
126
Decode Signal Stream / Serial-to-Parallel Converter
...
Data Out (Parallel Output)

FIG. 2A

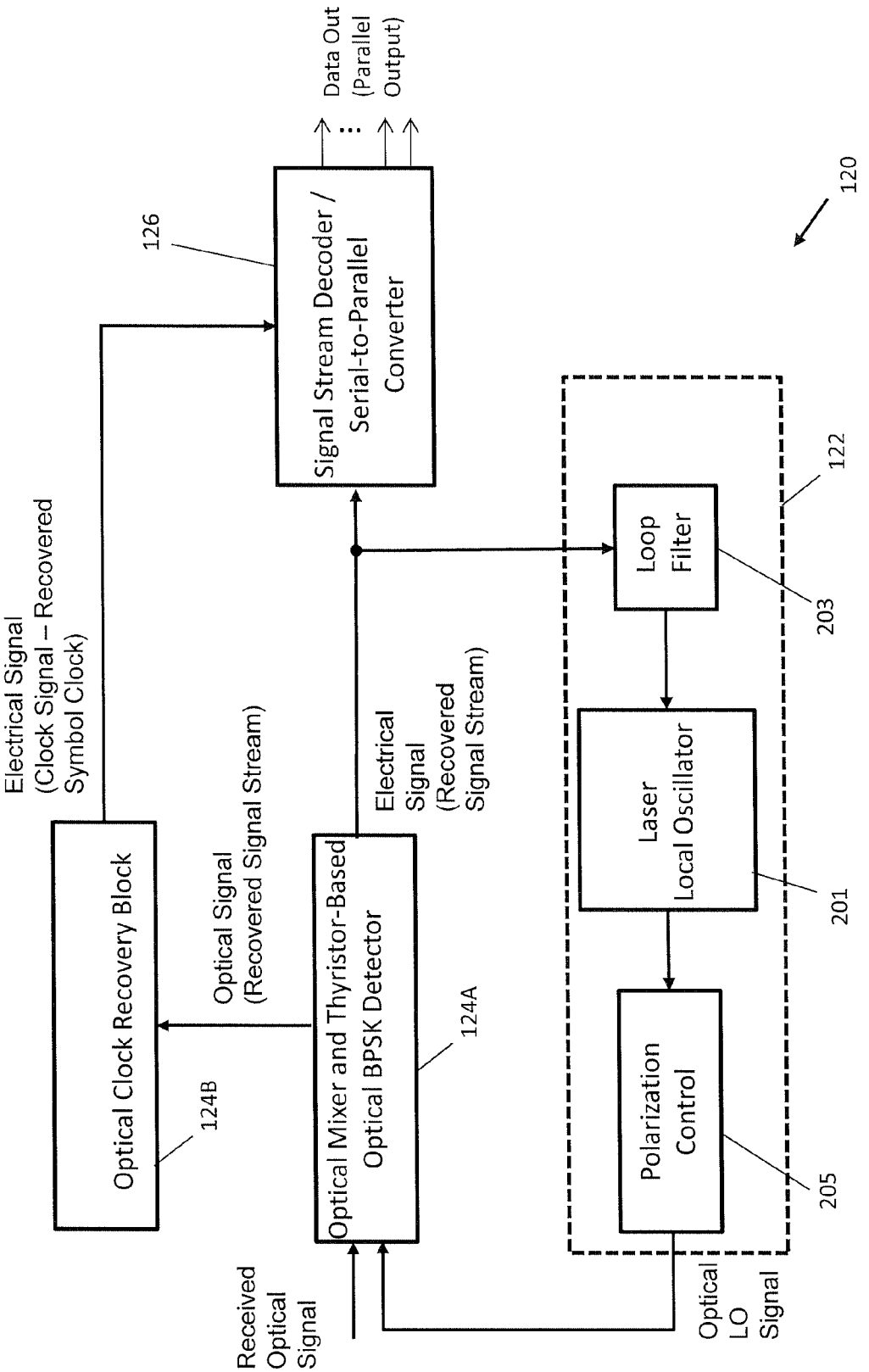

Data Out (Parallel Output)
126
Signal Stream Decoder / Serial-to-Parallel Converter
120
Electrical Signal (Clock Signal – Recovered Symbol Clock)
Loop Filter
122
203
Electrical Signal (Recovered Signal Stream)
Optical Signal (Recovered Signal Stream)
Laser Local Oscillator
Optical Clock Recovery Block
Optical Mixer and Thyristor-Based Optical BPSK Detector
124A
124B
201
Polarization Control
205
Received Optical Signal
Optical LO Signal

FIG. 2B

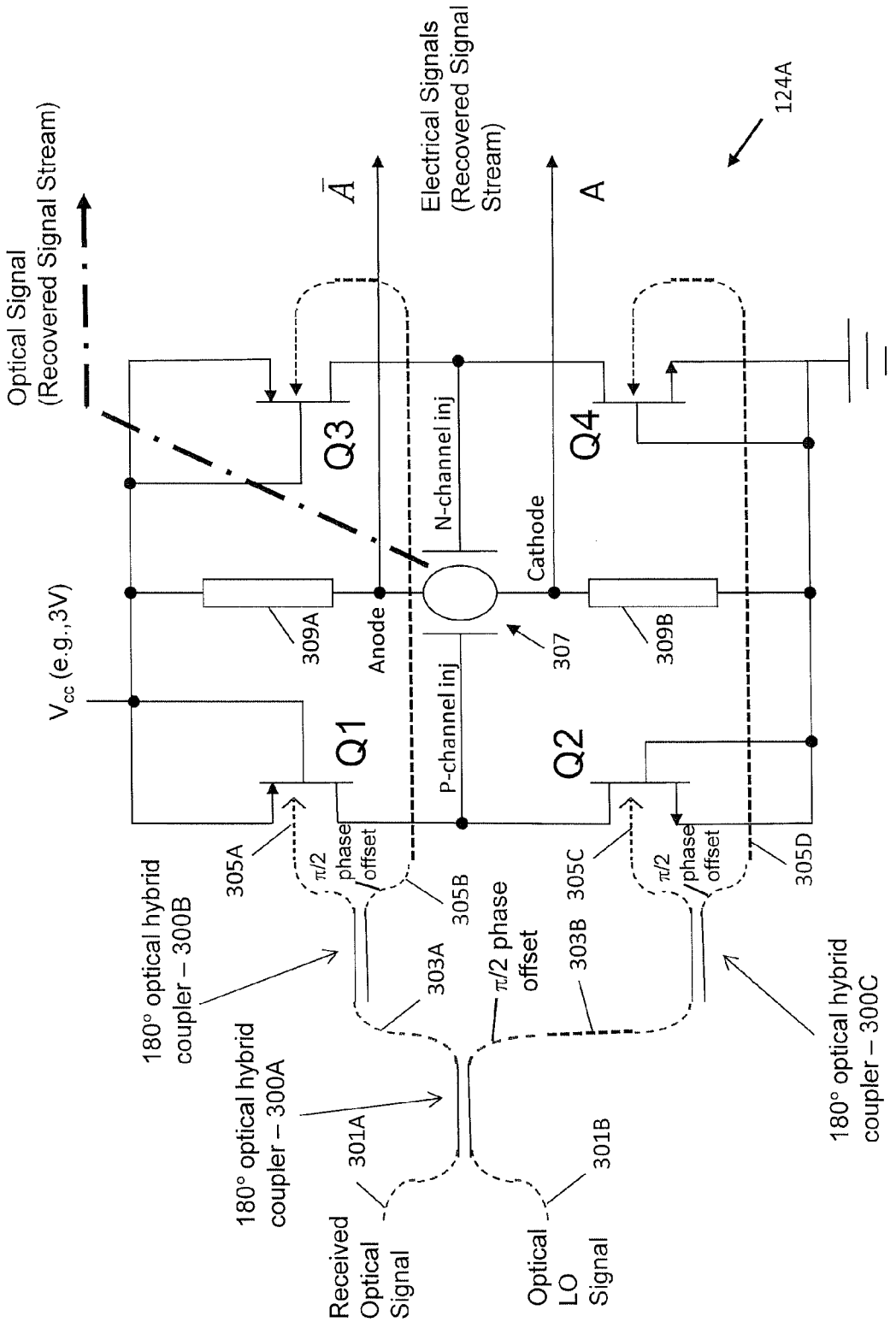

Optical Signal
(Recovered Signal Stream)
Electrical Signals
(Recovered Signal
Stream)
124A
$\bar{A}$
A
Q3
Q4
Q1
Q2
N-channel inj
P-channel inj
Cathode
Anode
307
309A
309B
V_{cc} (e.g.,3V)
305A
305B
305C
305D
$\pi/2$ phase offset
$\pi/2$ phase offset
303A
303B
$\pi/2$ phase offset
180° optical hybrid coupler – 300B
180° optical hybrid coupler – 300A
180° optical hybrid coupler – 300C
301A
301B
Received Optical Signal
Optical LO Signal

FIG. 3A

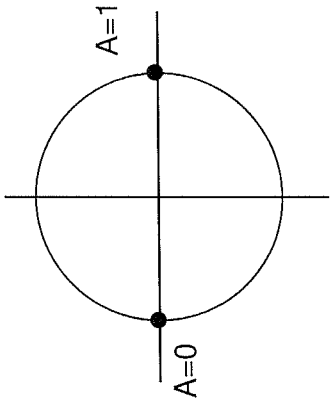


FIG. 3C

φ_s \ A	1	0
0		
π		

FIG. 3B

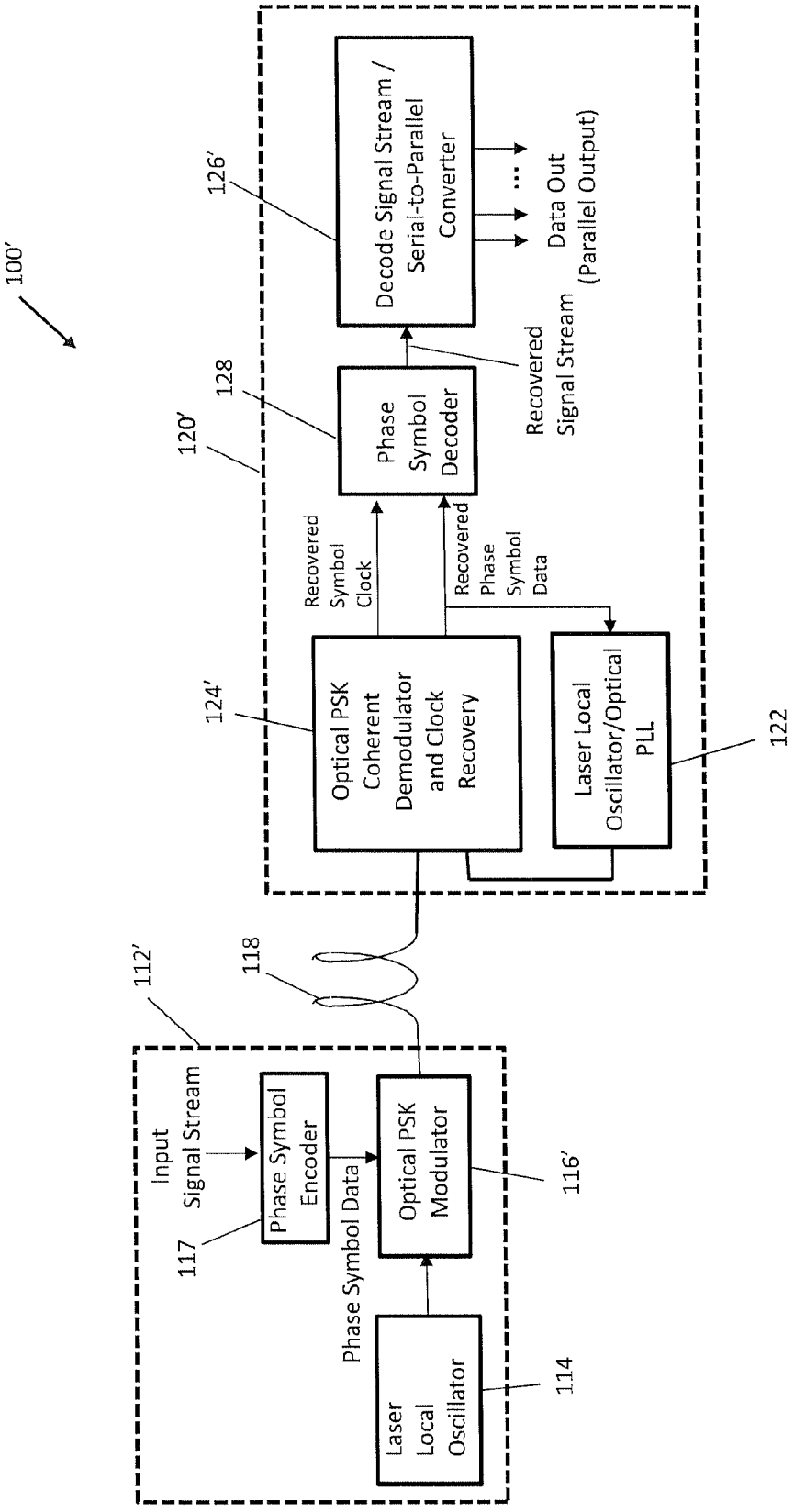

100'
112'
118
Input Signal Stream
117
Phase Symbol Encoder
Phase Symbol Data
Optical PSK Modulator
116'
Laser Local Oscillator
114
120'
124'
Optical PSK Coherent Demodulator and Clock Recovery
Recovered Symbol Clock
Recovered Phase Symbol Data
Laser Local Oscillator/Optical PLL
122
128
Phase Symbol Decoder
Recovered Signal Stream
126'
Decode Signal Stream / Serial-to-Parallel Converter
Data Out (Parallel Output)

FIG. 4

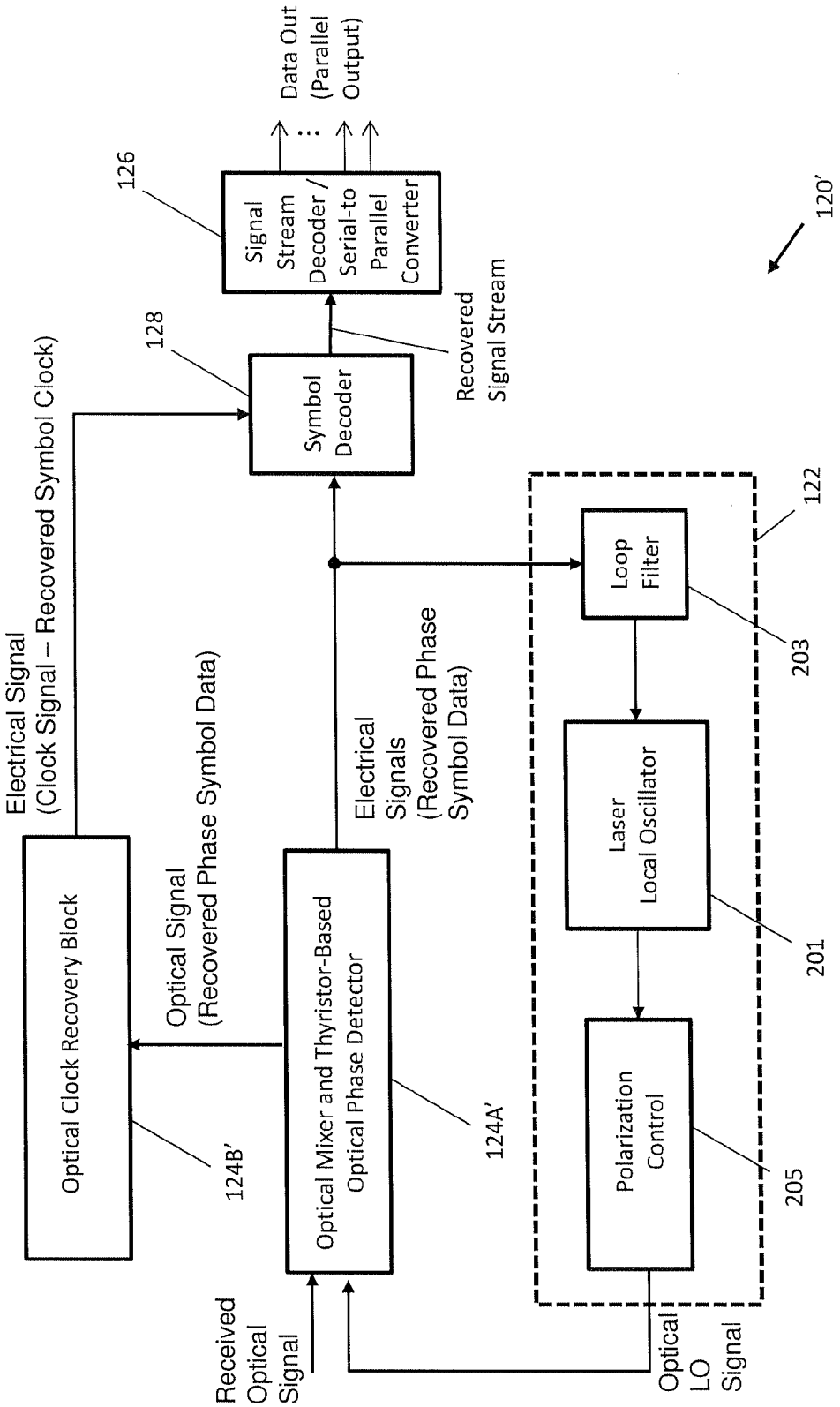

Data Out (Parallel Output)
126
Signal Stream Decoder / Serial-to Parallel Converter
120'
128
Symbol Decoder
Recovered Signal Stream
Electrical Signal (Clock Signal – Recovered Symbol Clock)
122
Loop Filter
203
Optical Signal (Recovered Phase Symbol Data)
Electrical Signals (Recovered Phase Symbol Data)
Laser Local Oscillator
201
Optical Clock Recovery Block
124B'
Optical Mixer and Thyristor-Based Optical Phase Detector
124A'
Polarization Control
205
Received Optical Signal
Optical LO Signal

FIG. 5

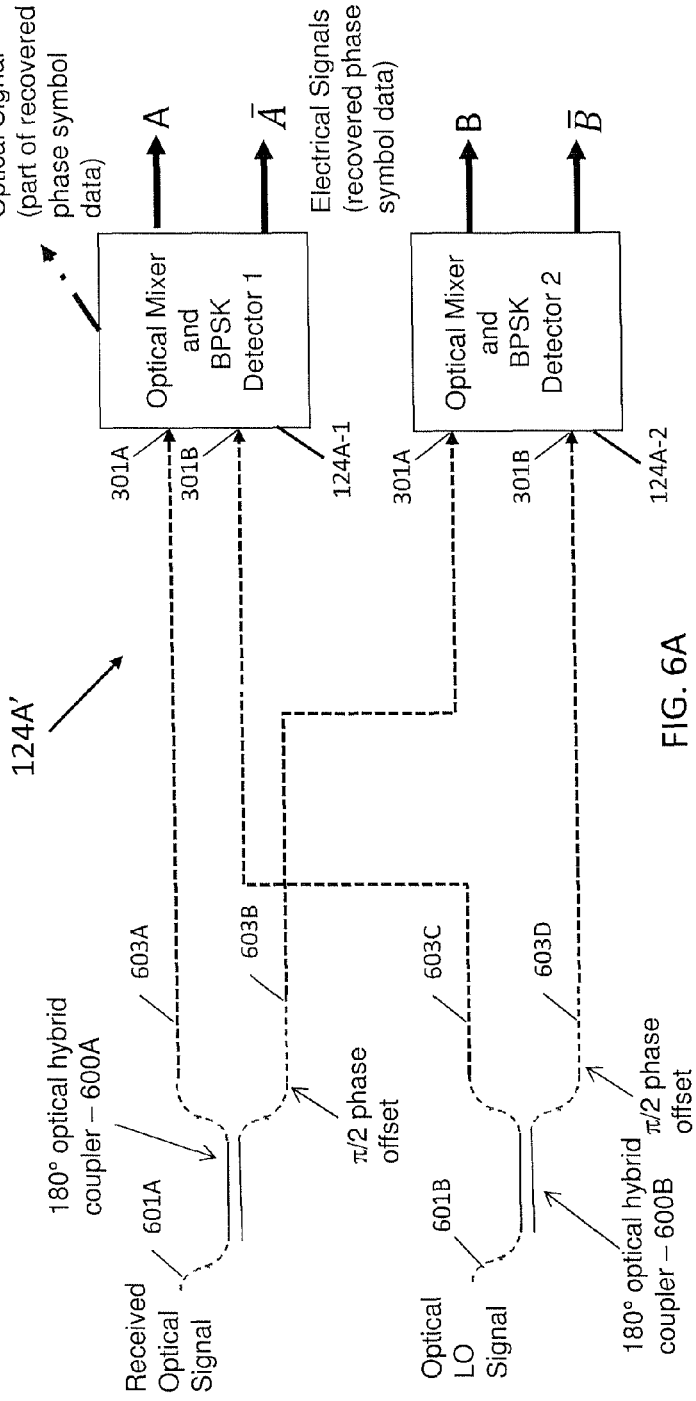


FIG. 6A

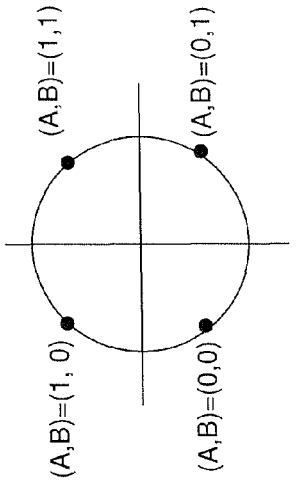


FIG. 6C

φ_s	A	B
$\pi/4$	1	1
$3\pi/4$	1	0
$5\pi/4$	0	0
$7\pi/4$	0	1

FIG. 6B

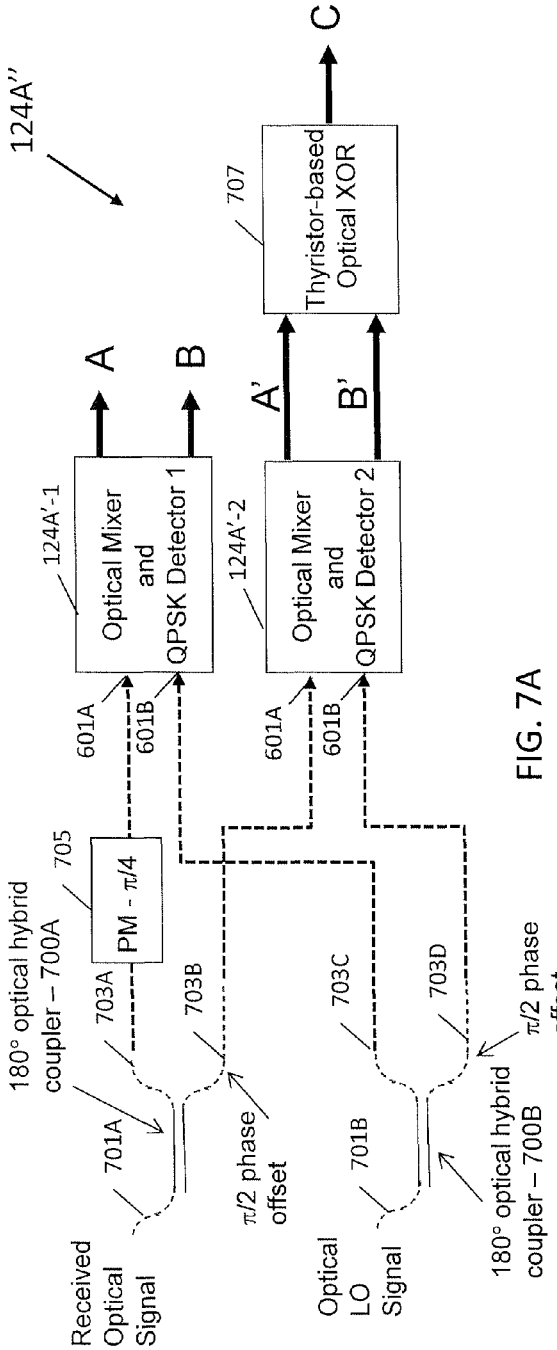


FIG. 7A

φ_s	A	B	A'	B'	C
0	0	0	0	0	0
$\pi/4$	1	0	0	0	0
$\pi/2$	1	0	1	0	1
$3\pi/4$	1	1	1	0	1
π	1	1	1	1	0
$5\pi/4$	0	1	1	1	0
$3\pi/2$	0	1	0	1	1
$7\pi/4$	0	0	0	1	1

FIG. 7B

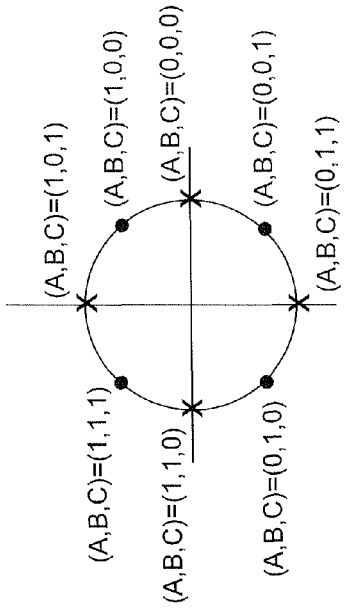


FIG. 7C

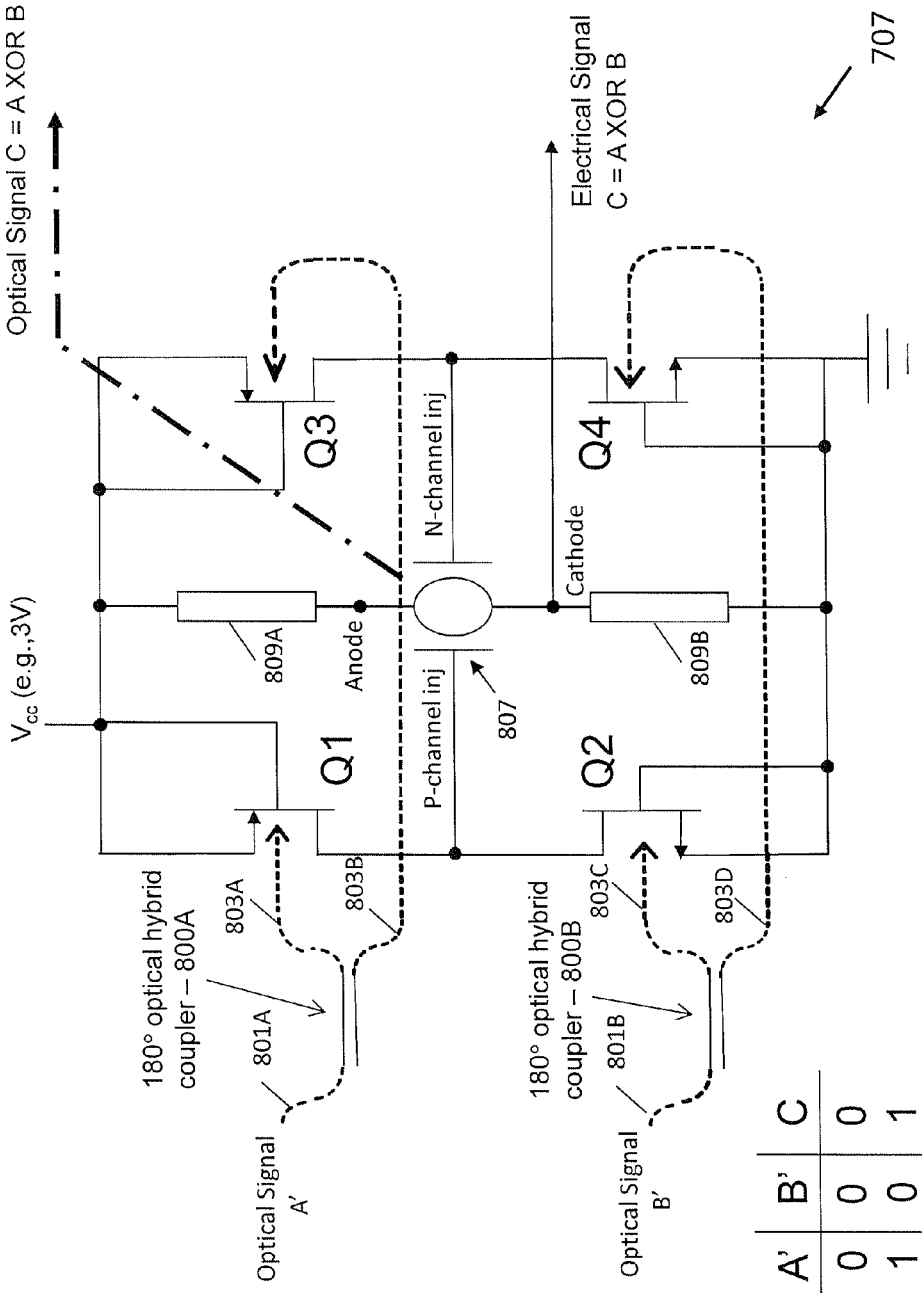


FIG. 8A

A'	B'	C
0	0	0
1	0	1
0	1	1
1	1	0

FIG. 8B

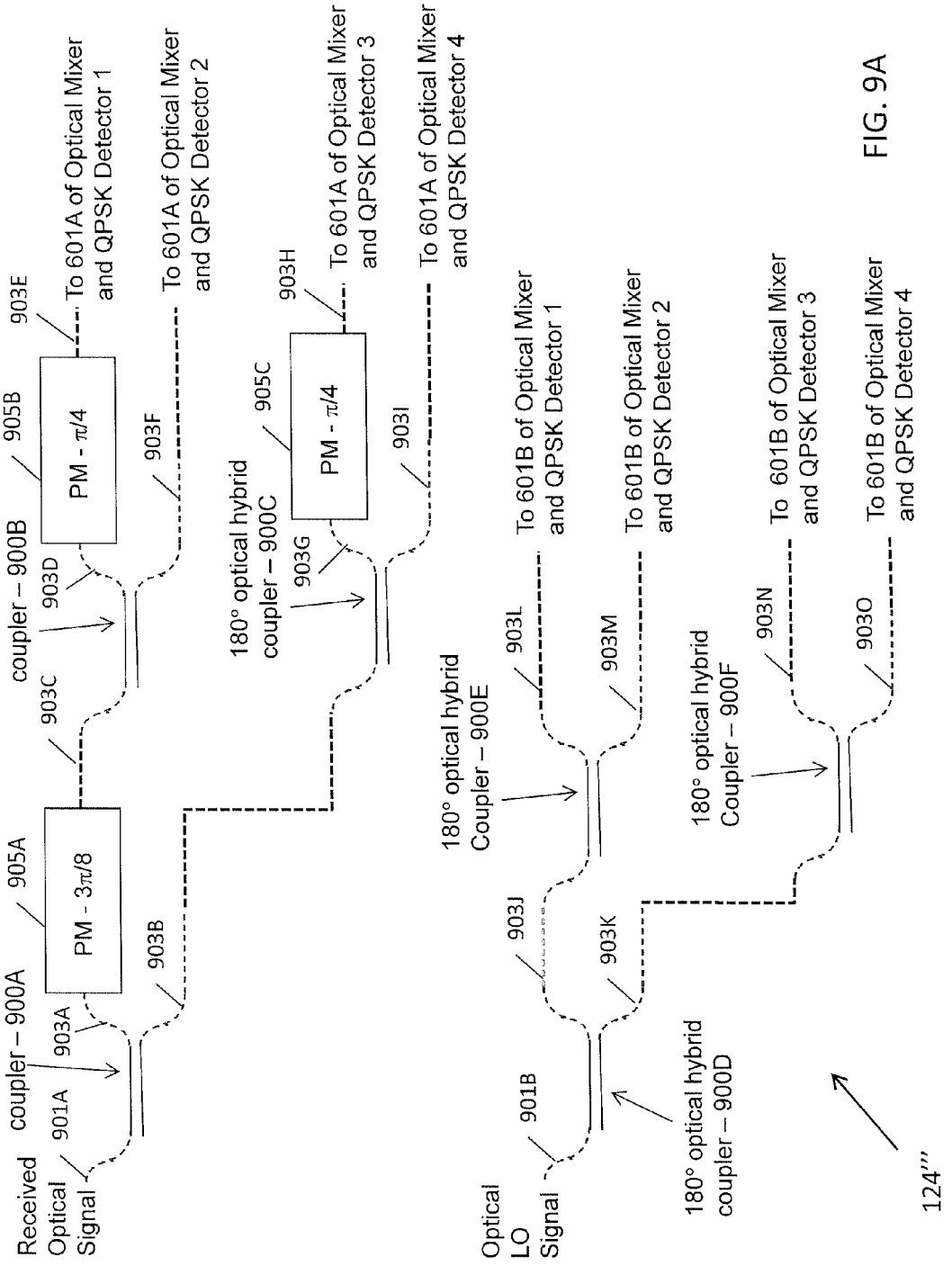

Received Optical Signal
901A
180° optical hybrid coupler – 900A
903A
905A
PM - 3π/8
903B
903C
180° optical hybrid coupler – 900B
905B
PM - π/4
903D
903E
To 601A of Optical Mixer and QPSK Detector 1
903F
To 601A of Optical Mixer and QPSK Detector 2
180° optical hybrid coupler – 900C
903G
905C
PM - π/4
903H
To 601A of Optical Mixer and QPSK Detector 3
903I
To 601A of Optical Mixer and QPSK Detector 4
Optical LO Signal
901B
180° optical hybrid coupler – 900D
903J
903K
180° optical hybrid Coupler – 900E
903L
To 601B of Optical Mixer and QPSK Detector 1
903M
To 601B of Optical Mixer and QPSK Detector 2
180° optical hybrid Coupler – 900F
903N
To 601B of Optical Mixer and QPSK Detector 3
903O
To 601B of Optical Mixer and QPSK Detector 4
124'''

FIG. 9A

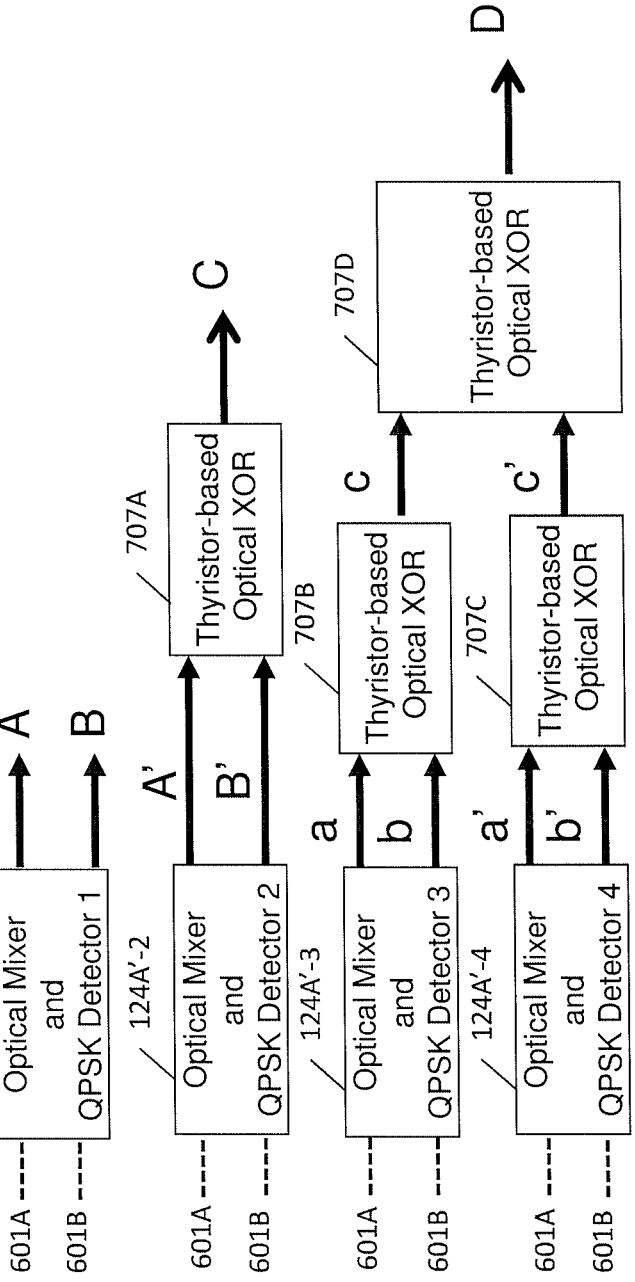

124A'-1
Optical Mixer and QPSK Detector 1
601A
601B
A
B
124A'-2
Optical Mixer and QPSK Detector 2
A'
B'
707A
Thyristor-based Optical XOR
C
124A'-3
Optical Mixer and QPSK Detector 3
a
b
707B
Thyristor-based Optical XOR
c
124A'-4
Optical Mixer and QPSK Detector 4
a'
b'
707C
Thyristor-based Optical XOR
c'
707D
Thyristor-based Optical XOR
D

FIG. 9B

φ_s	A	B	A'	B'	C	a	b	c	a'	b'	c'	D
0	0	1	0	1	1	0	1	1	0	1	1	0
π/8	0	0	0	1	1	0	1	1	0	1	1	0
π/4	0	0	0	1	1	0	0	0	0	1	1	1
3π/8	0	0	0	0	0	0	0	0	0	1	1	1
π/2	0	0	0	0	0	0	0	0	0	0	0	0
5π/8	1	0	0	0	0	0	0	0	0	0	0	0
3π/4	1	0	0	0	0	1	0	1	0	0	0	1
7π/8	1	0	1	0	1	1	0	1	0	0	0	1
π	1	0	1	0	1	1	0	1	1	0	1	0
9π/8	1	1	1	0	1	1	0	1	1	0	1	0
5π/4	1	1	1	0	1	1	1	0	1	0	1	1
11π/8	1	1	1	1	0	1	1	0	1	0	1	1
3π/2	1	1	1	1	0	1	1	0	1	1	0	0
13π/8	0	1	1	1	0	1	1	0	1	1	0	0
7π/4	0	1	1	1	0	0	1	1	1	1	0	1
15π/8	0	1	0	1	1	0	1	1	1	1	0	1

FIG. 9C

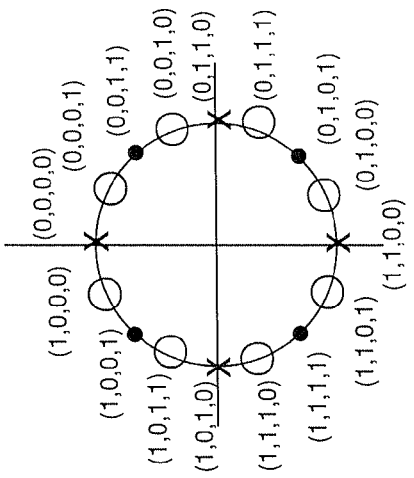


FIG. 9D

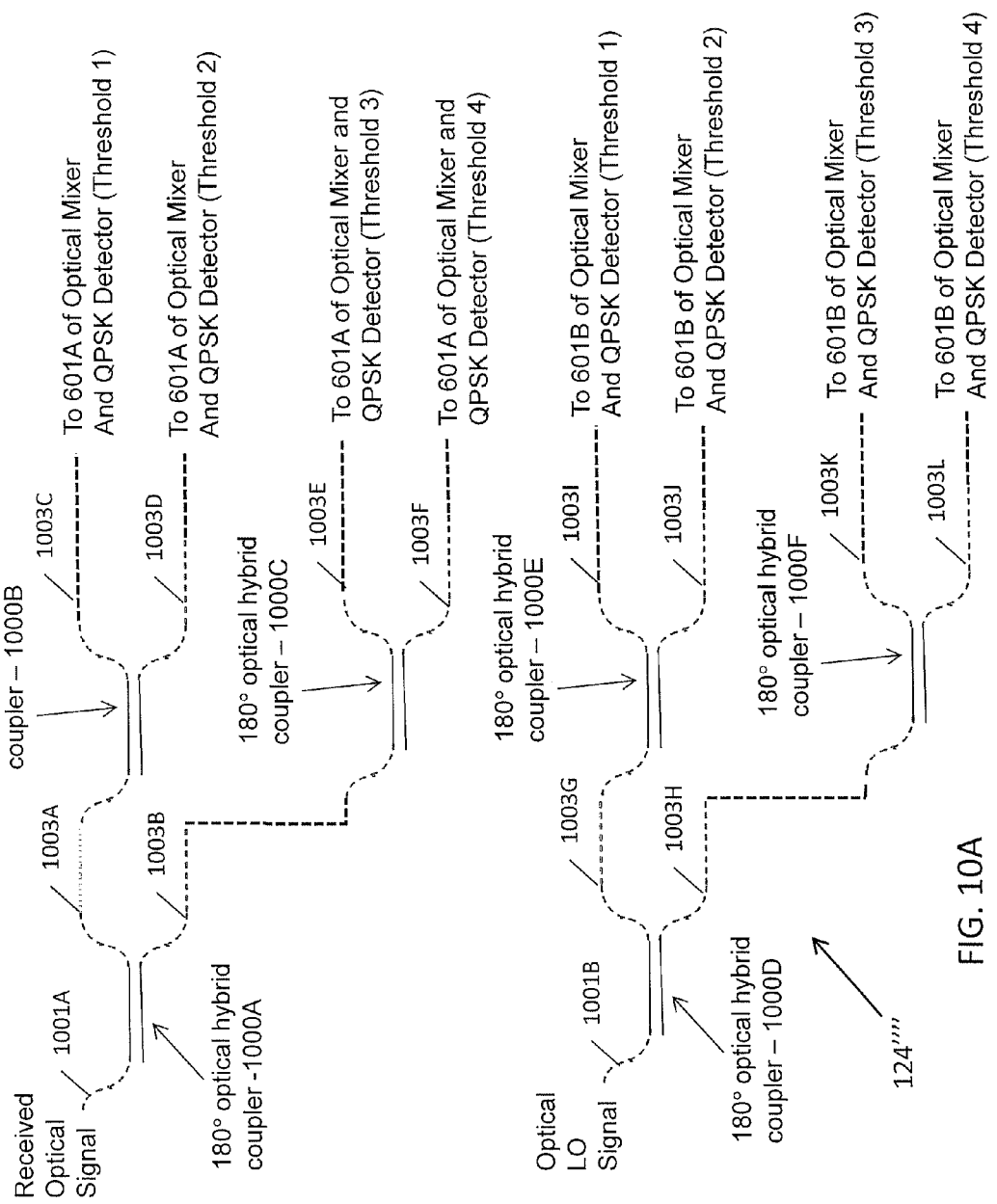

Received Optical Signal
1001A
180° optical hybrid coupler -1000A
1003A
1003B
180° optical hybrid coupler – 1000B
1003C
To 601A of Optical Mixer And QPSK Detector (Threshold 1)
1003D
To 601A of Optical Mixer And QPSK Detector (Threshold 2)
180° optical hybrid coupler – 1000C
1003E
To 601A of Optical Mixer and QPSK Detector (Threshold 3)
1003F
To 601A of Optical Mixer and QPSK Detector (Threshold 4)
Optical LO Signal
1001B
180° optical hybrid coupler – 1000D
1003G
1003H
180° optical hybrid coupler – 1000E
1003I
To 601B of Optical Mixer And QPSK Detector (Threshold 1)
1003J
To 601B of Optical Mixer And QPSK Detector (Threshold 2)
180° optical hybrid coupler – 1000F
1003K
To 601B of Optical Mixer And QPSK Detector (Threshold 3)
1003L
To 601B of Optical Mixer And QPSK Detector (Threshold 4)
124''''

FIG. 10A

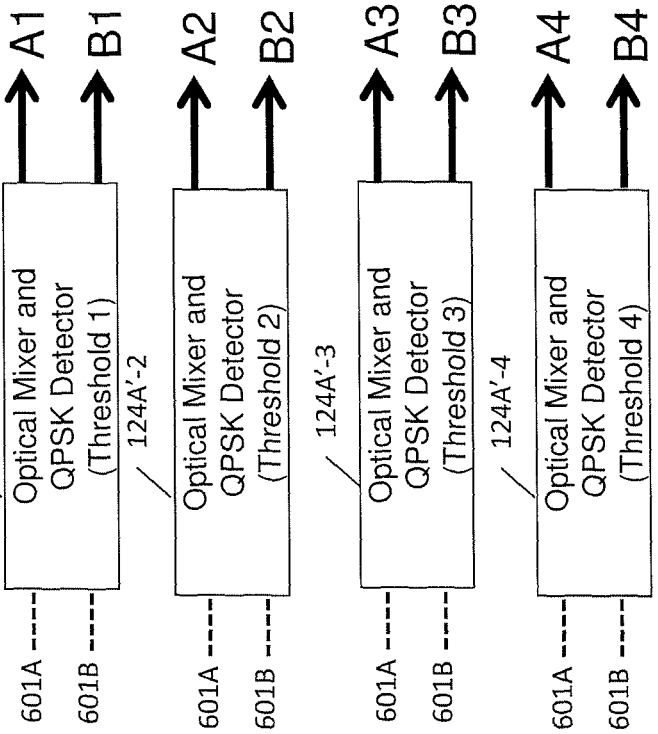

124A'-1
Optical Mixer and QPSK Detector (Threshold 1)
A1
B1
601A
601B
124A'-2
Optical Mixer and QPSK Detector (Threshold 2)
A2
B2
601A
601B
124A'-3
Optical Mixer and QPSK Detector (Threshold 3)
A3
B3
601A
601B
124A'-4
Optical Mixer and QPSK Detector (Threshold 4)
A4
B4
601A
601B

FIG. 10B

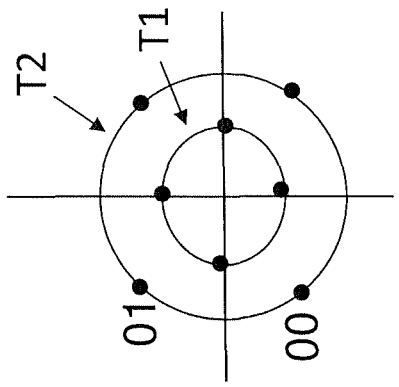


FIG. 10D

Φ_s (T)	A1	B1	A2	B2
0 (T1)	1	0		
π/4 (T2)			1	1
π/2 (T1)	1	1		
3π/4 (T2)			0	1
π (T1)	0	1		
5π/4 (T2)			0	0
3π/2(T1)	0	0		
7π/4(T2)			1	0

FIG. 10C

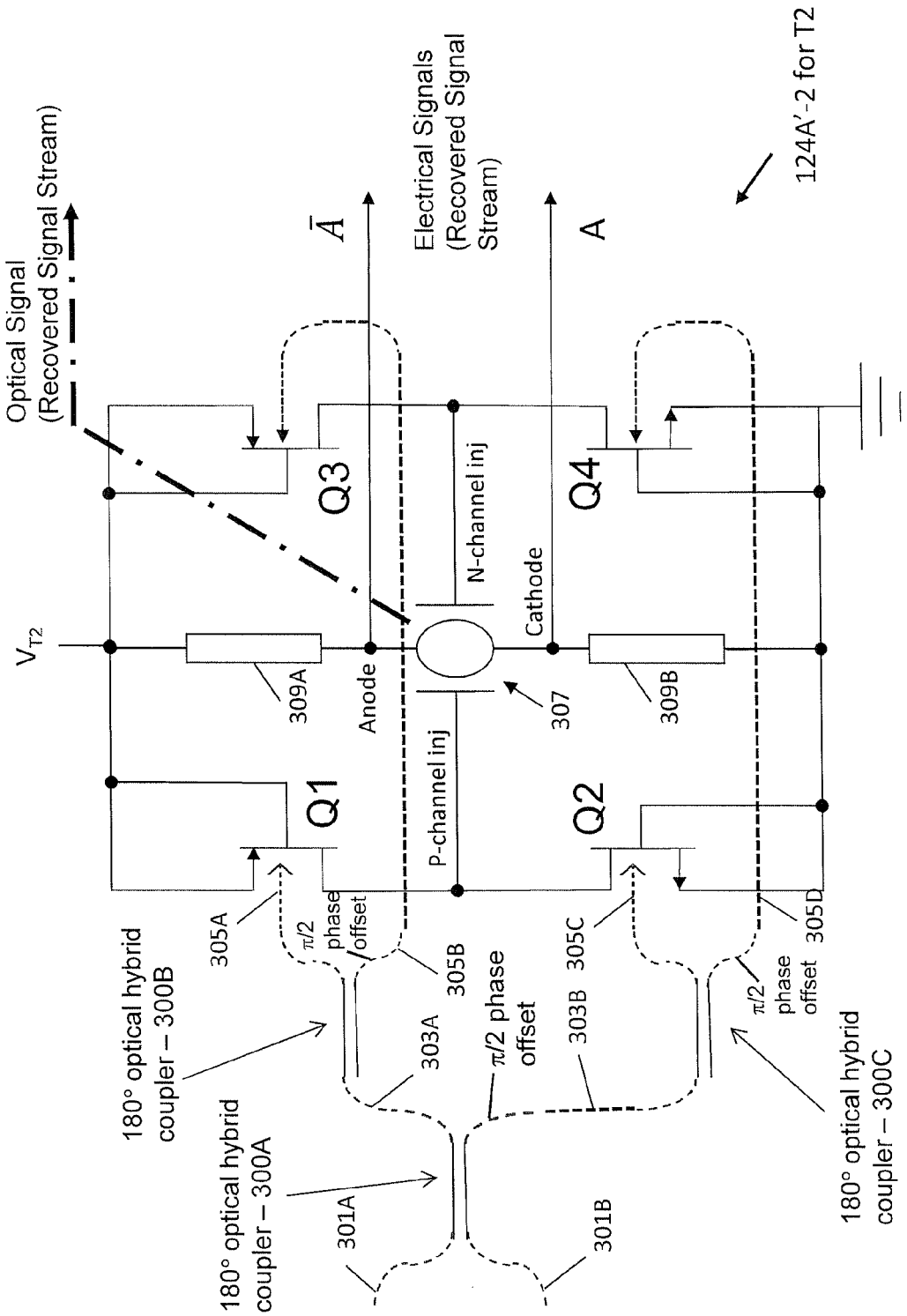

Optical Signal
(Recovered Signal Stream)
V_{T2}
180° optical hybrid coupler – 300B
180° optical hybrid coupler – 300A
180° optical hybrid coupler – 300C
Q1
Q2
Q3
Q4
P-channel inj
N-channel inj
Anode
Cathode
307
309A
309B
305A
305B
305C
305D
303A
303B
301A
301B
$\pi/2$ phase offset
Electrical Signals (Recovered Signal Stream)
$\bar{A}$
A
124A'-2 for T2

FIG. 10E

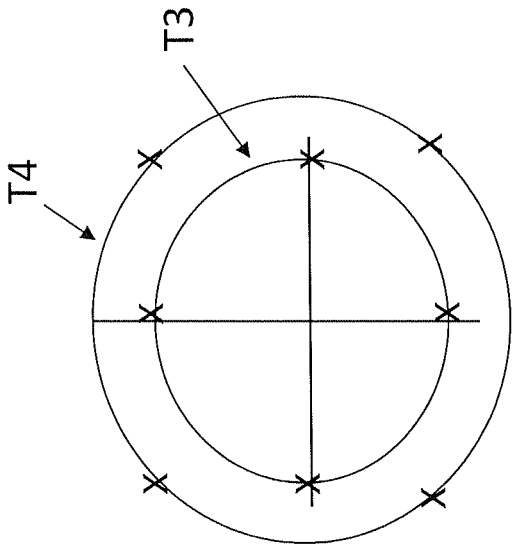


FIG. 10G

Φ_s (T)	A3	B3	A4	B4
0 (T3)	1	0		
π/4 (T4)			1	1
π/2 (T3)	1	1		
3π/4 (T4)			0	1
π (T3)	0	1		
5π/4 (T4)			0	0
3π/2(T3)	0	0		
7π/4(T4)			1	0

FIG. 10F

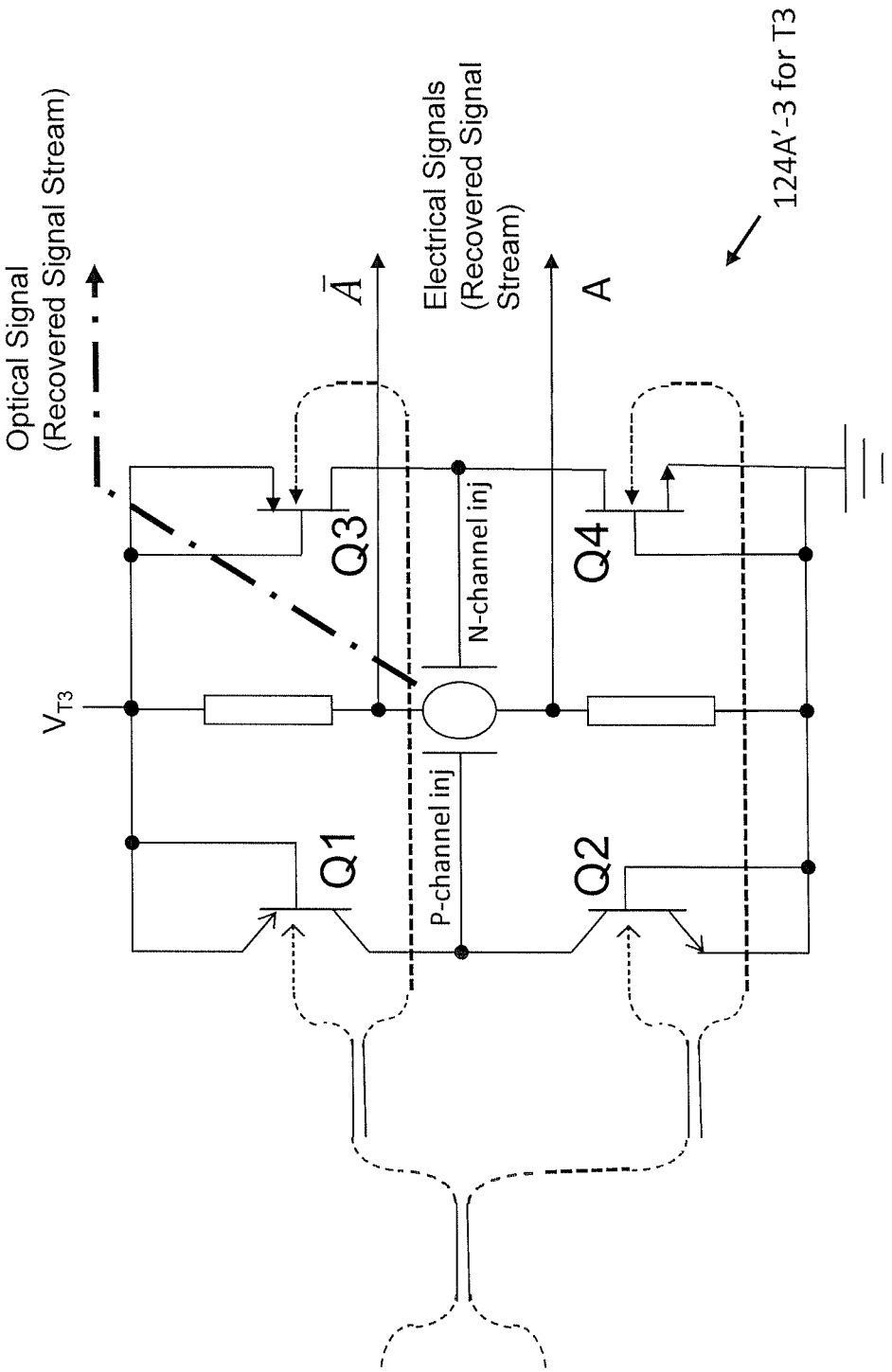

Optical Signal
(Recovered Signal Stream)
$\bar{A}$
Electrical Signals
(Recovered Signal
Stream)
A
124A'-3 for T3
Q3
N-channel inj
Q4
V_{T3}
P-channel inj
Q1
Q2

FIG. 10H

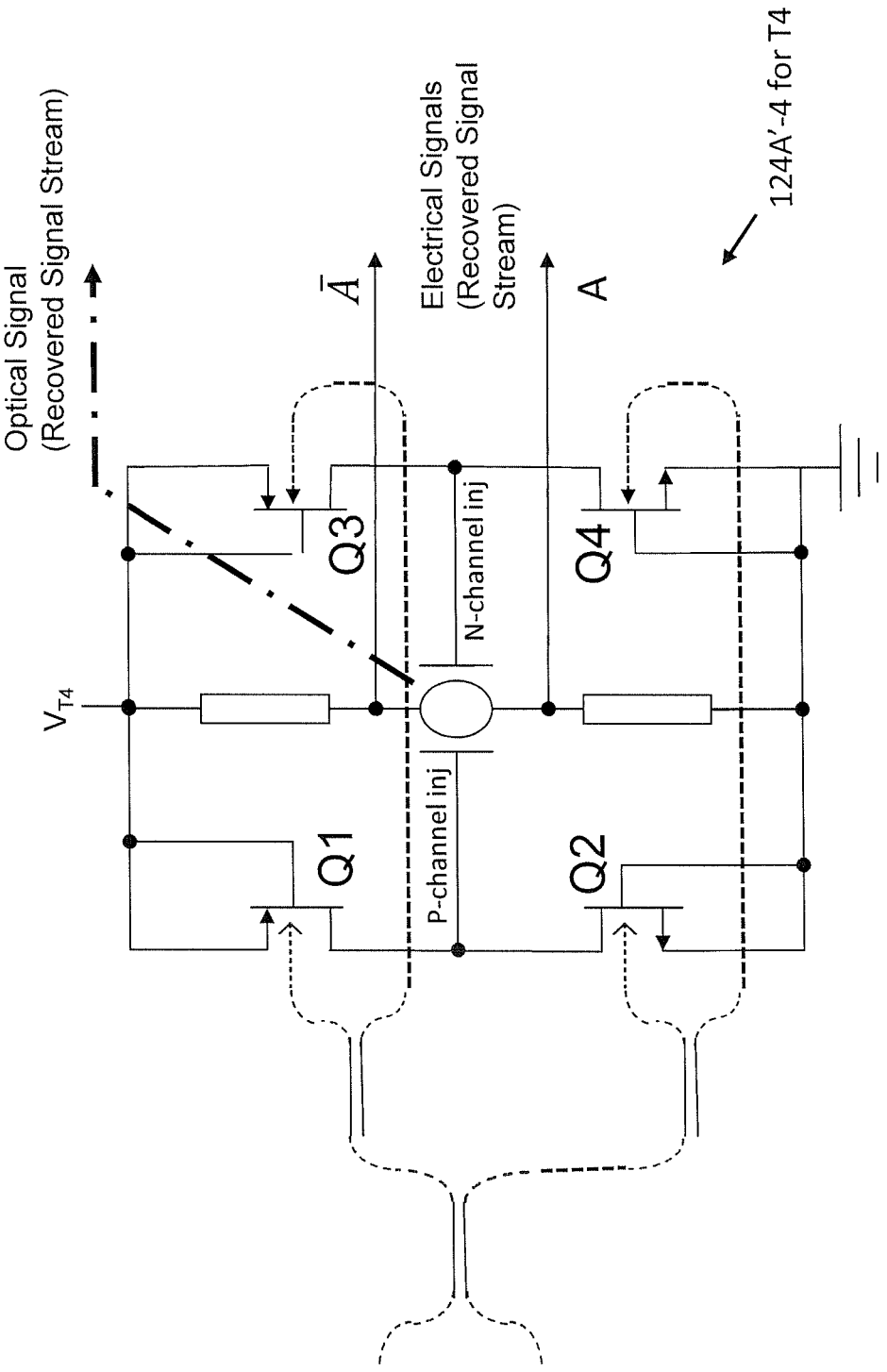

Optical Signal
(Recovered Signal Stream)
$\bar{A}$
Electrical Signals
(Recovered Signal
Stream)
A
124A'-4 for T4
Q3
N-channel inj
Q4
V_{T4}
Q1
P-channel inj
Q2

FIG. 10I

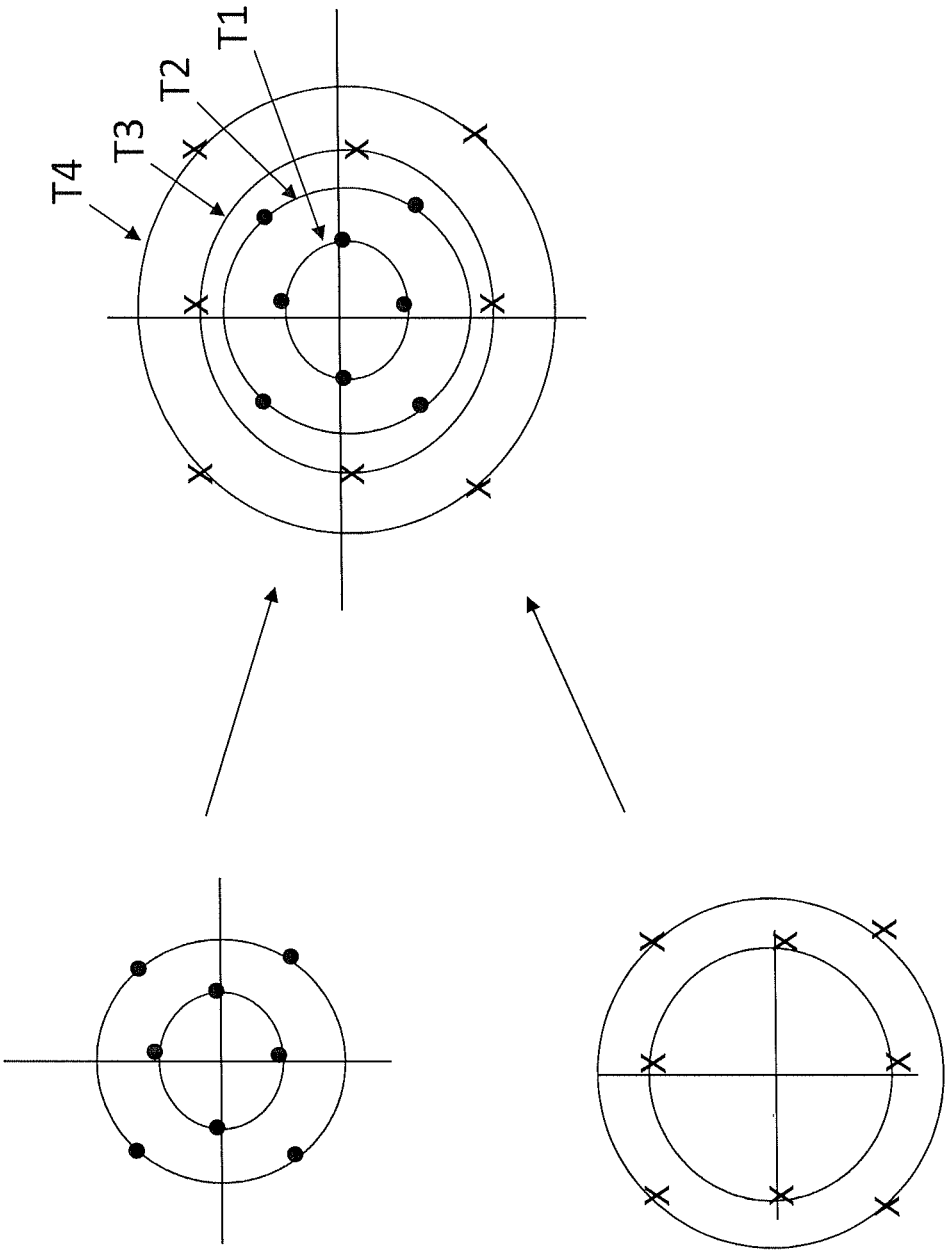


FIG. 10J

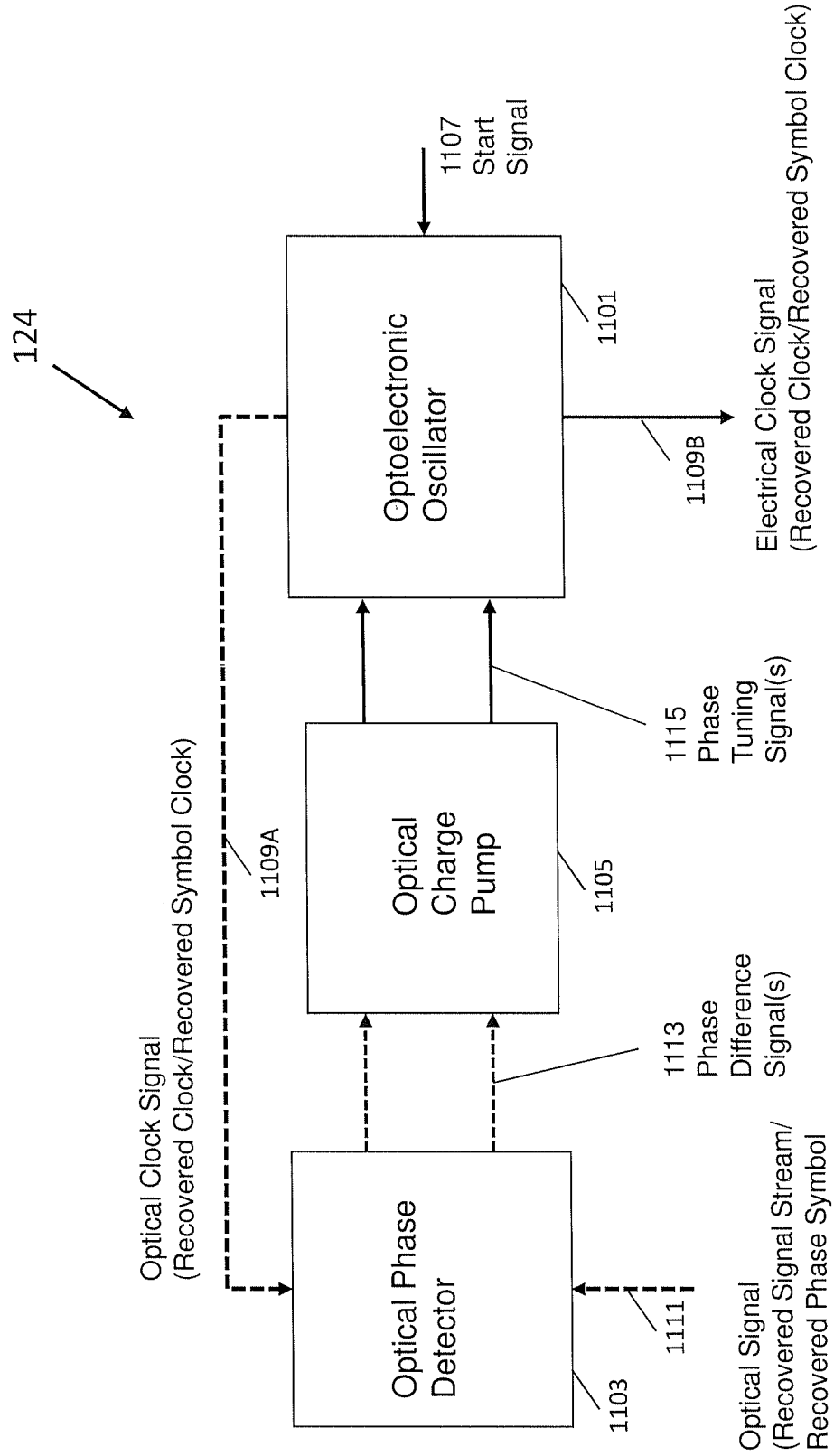

124
Optoelectronic Oscillator
1101
1107 Start Signal
1109B
Electrical Clock Signal (Recovered Clock/Recovered Symbol Clock)
Optical Charge Pump
1105
1115 Phase Tuning Signal(s)
1109A
Optical Clock Signal (Recovered Clock/Recovered Symbol Clock)
Optical Phase Detector
1103
1111
1113 Phase Difference Signal(s)
Optical Signal (Recovered Signal Stream/ Recovered Phase Symbol Data)

FIG. 11

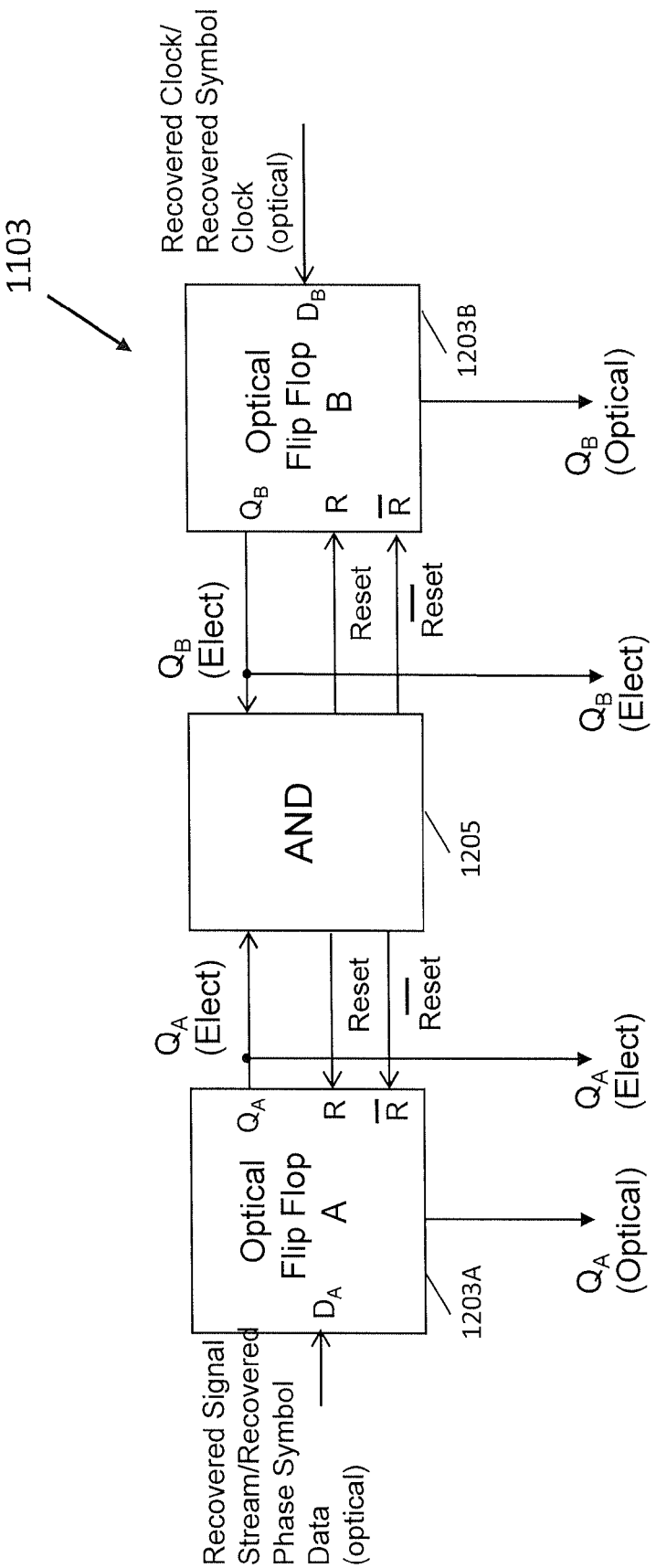

1103
Recovered Clock/
Recovered Symbol
Clock
(optical)
Optical
Flip Flop
B
1203B
D_B
Q_B
R
$\overline{R}$
Q_B
(Optical)
Q_B
(Elect)
Reset
$\overline{Reset}$
Q_B
(Elect)
AND
1205
Q_A
(Elect)
Reset
$\overline{Reset}$
Q_A
(Elect)
Optical
Flip Flop
A
1203A
D_A
Q_A
R
$\overline{R}$
Q_A
(Optical)
Recovered Signal
Stream/Recovered
Phase Symbol
Data
(optical)
to Charge Pump

FIG. 12A

Reset (input)	$\overline{Reset}$ (input)	Recovered Optical Signal D_A (input)	Q_A (output)	$\overline{Q_A}$ (output)
1	0	x	0	1
0	1	0	0	1
0	1	1	1	0

FIG. 12B

Reset (input)	$\overline{Reset}$ (input)	Optical Clock Signal D_B (input)	Q_B (output)	$\overline{Q_B}$ (output)
1	0	x	0	1
0	1	0	0	1
0	1	1	1	0

FIG. 12C

Q_A (input)	Q_B (input)	Reset (output)	$\overline{Reset}$ (output)
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

FIG. 12D

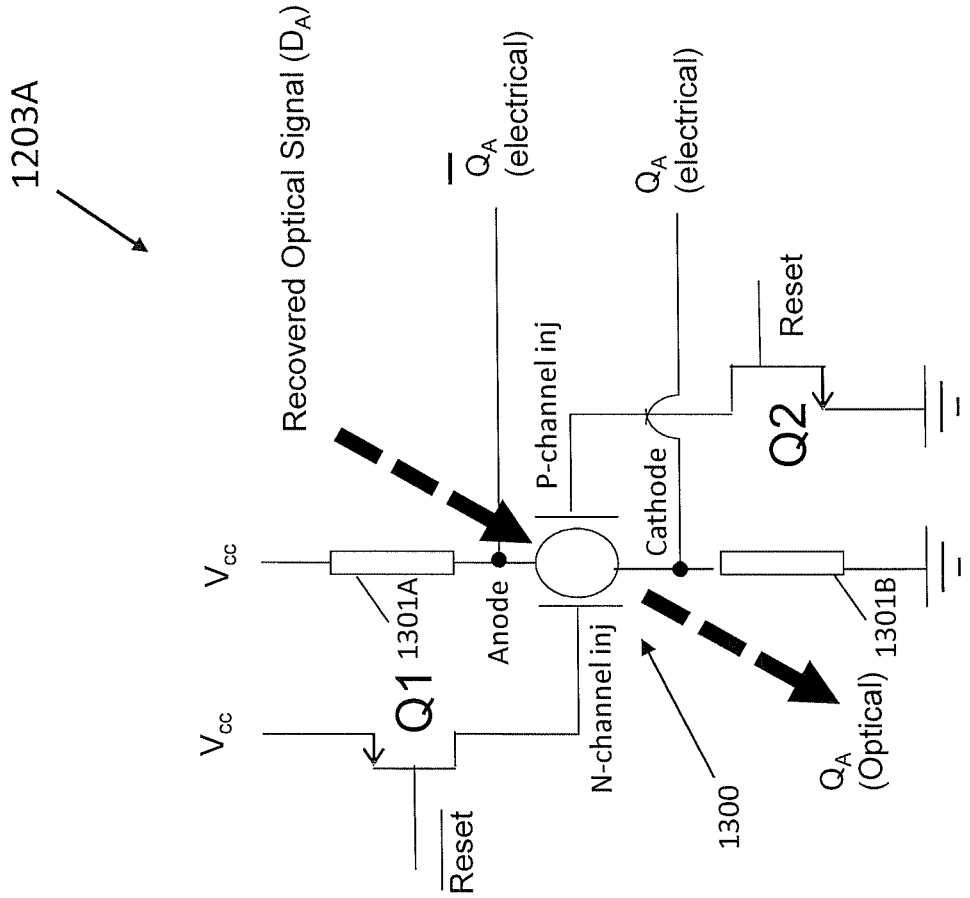

1203A
Recovered Optical Signal (D_A)
$\overline{Q_A}$ (electrical)
Q_A (electrical)
P-channel inj
Reset
Q2
Cathode
V_{cc}
1301A
Anode
Q1
V_{cc}
N-channel inj
1300
Q_A (Optical)
1301B
$\overline{Reset}$

FIG. 13A

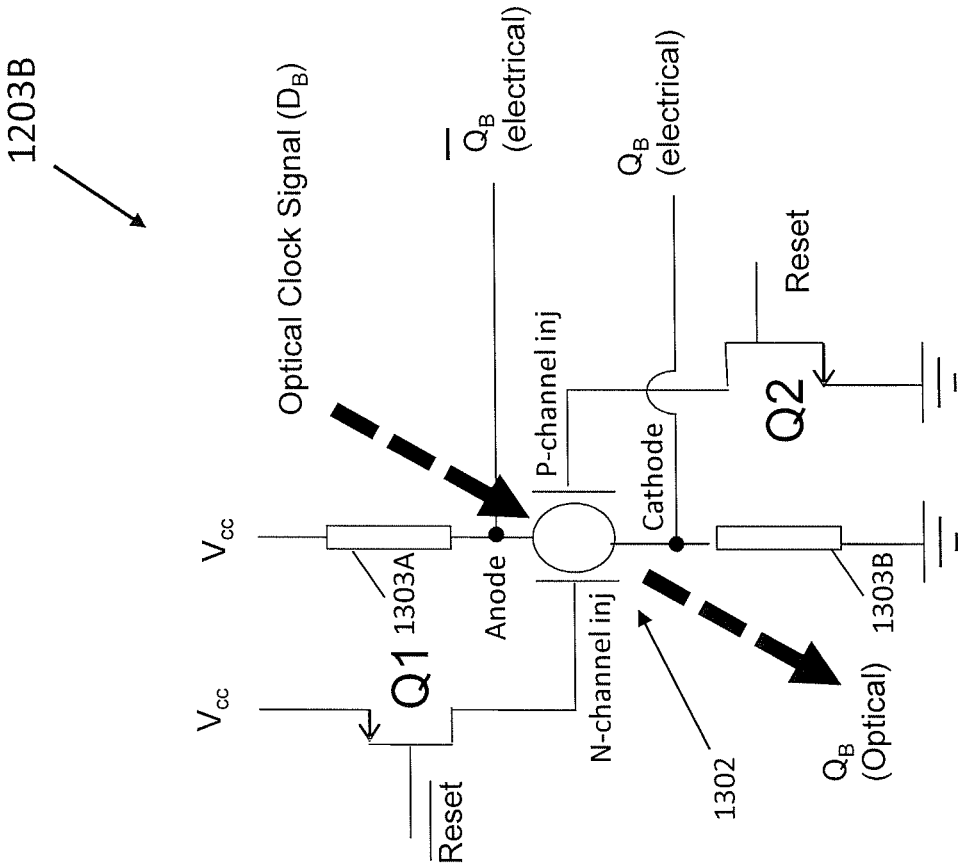

1203B
Optical Clock Signal (D_B)
$\overline{Q_B}$ (electrical)
Q_B (electrical)
Reset
P-channel inj
Cathode
Q2
V_{cc}
1303A
Anode
Q1
V_{cc}
N-channel inj
1302
Q_B (Optical)
1303B
Reset

FIG. 13B

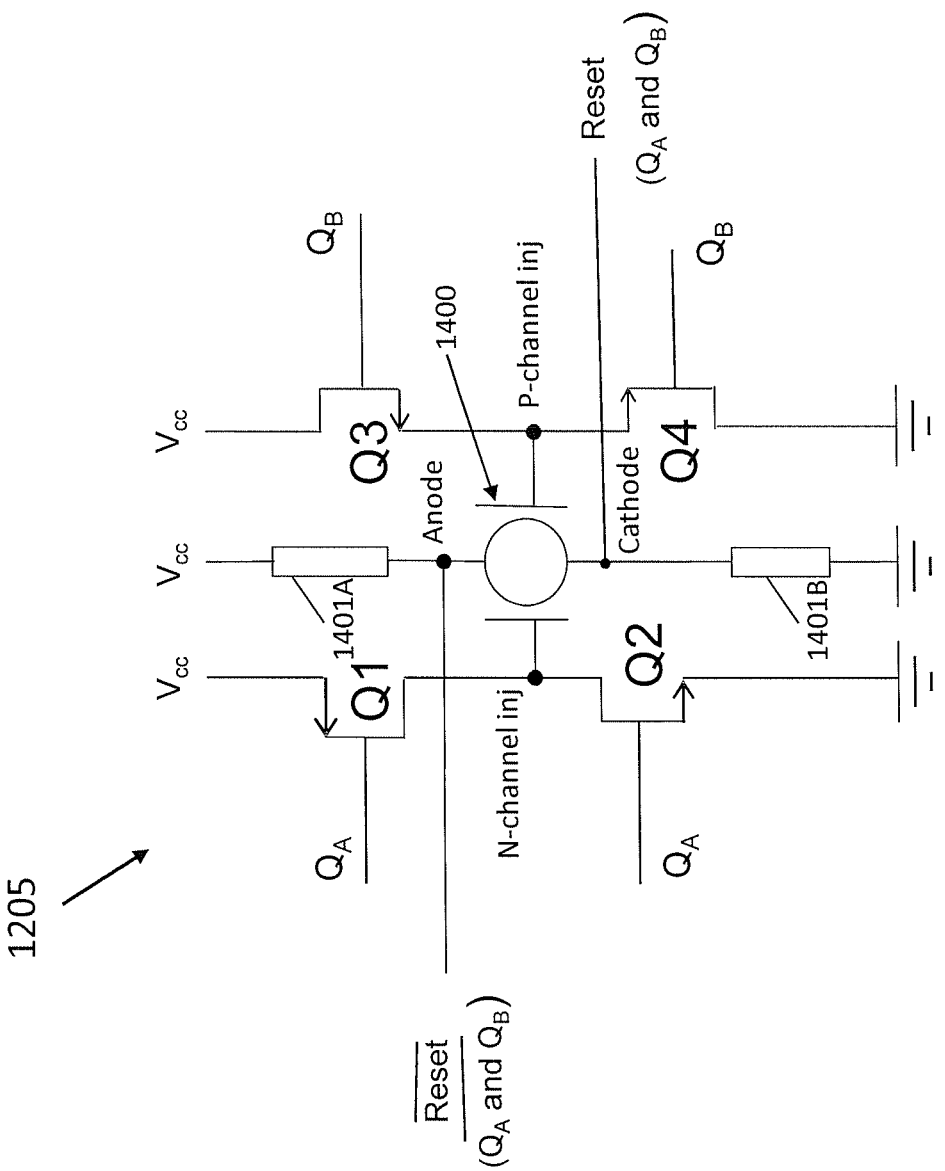

1205
V_{cc}
V_{cc}
V_{cc}
Q1
Q2
Q3
Q4
1401A
1401B
1400
Anode
Cathode
P-channel inj
N-channel inj
Reset
(Q_A and Q_B)
$\overline{\text{Reset}}$
(Q_A and Q_B)
Q_B
Q_B
Q_A
Q_A

FIG. 14A

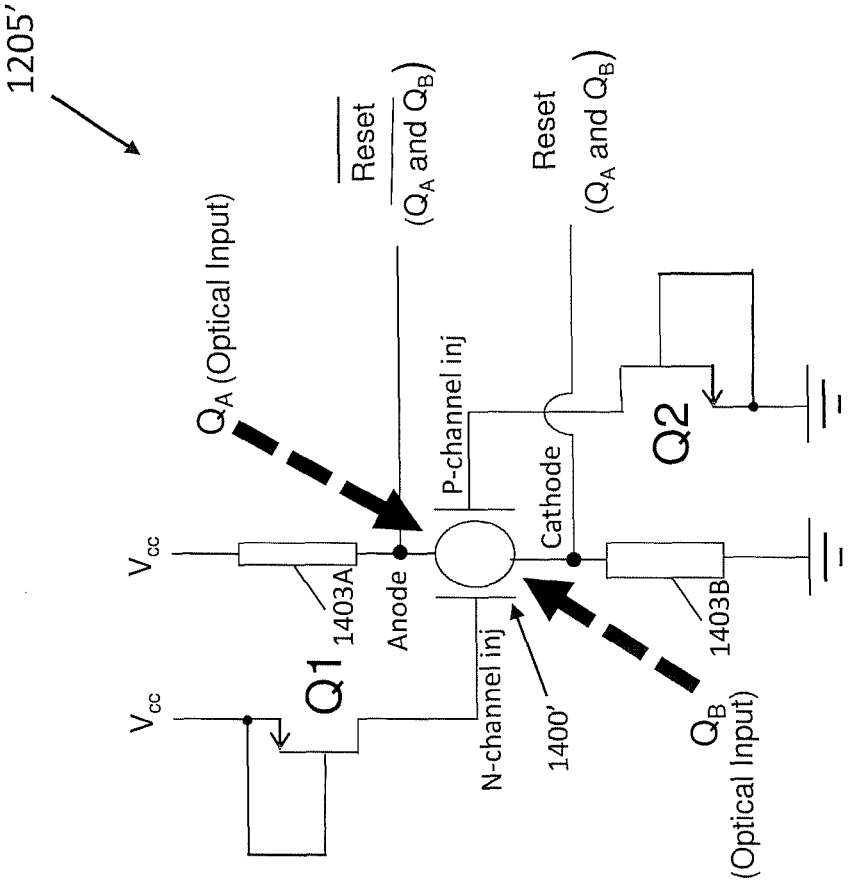
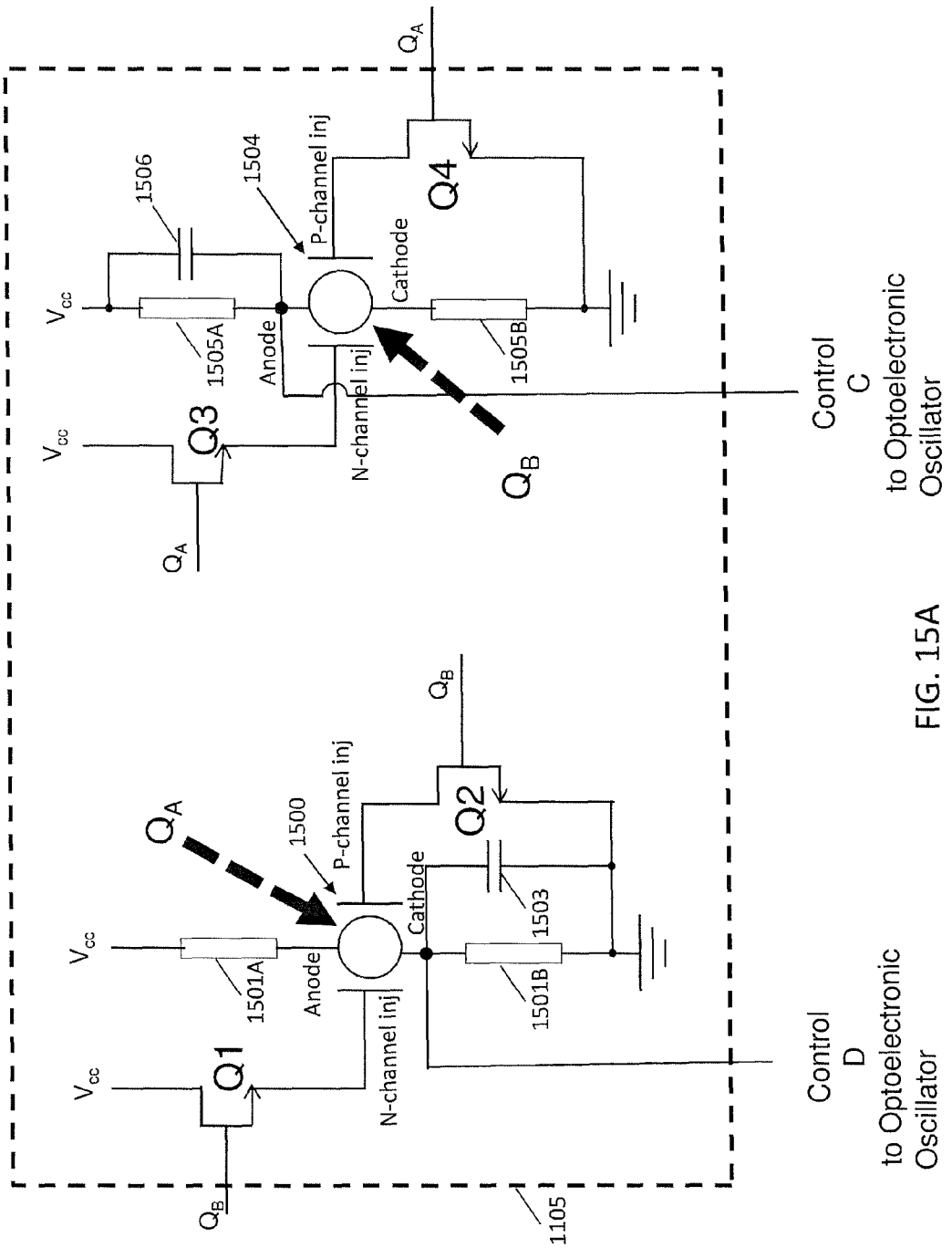

1205'
$\overline{\text{Reset}}$ (Q_A and Q_B)
Reset (Q_A and Q_B)
Q_A (Optical Input)
P-channel inj
V_{cc}
1403A
Anode
Cathode
Q2
Q1
N-channel inj
1400'
1403B
V_{cc}
Q_B (Optical Input)

FIG. 14B



Q_A
1506
1504
P-channel inj
Q4
Cathode
V_{cc}
1505A
Anode
1505B
N-channel inj
Q3
Q_B
Control
C
to Optoelectronic
Oscillator
Q_B
Q_A
1500
P-channel inj
Q2
Cathode
1503
V_{cc}
1501A
Anode
1501B
N-channel inj
Q1
Control
D
to Optoelectronic
Oscillator
1105

FIG. 15A

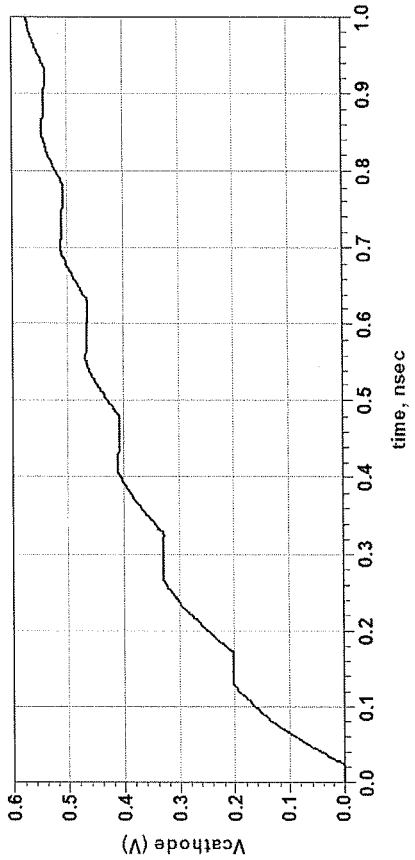


FIG. 15B

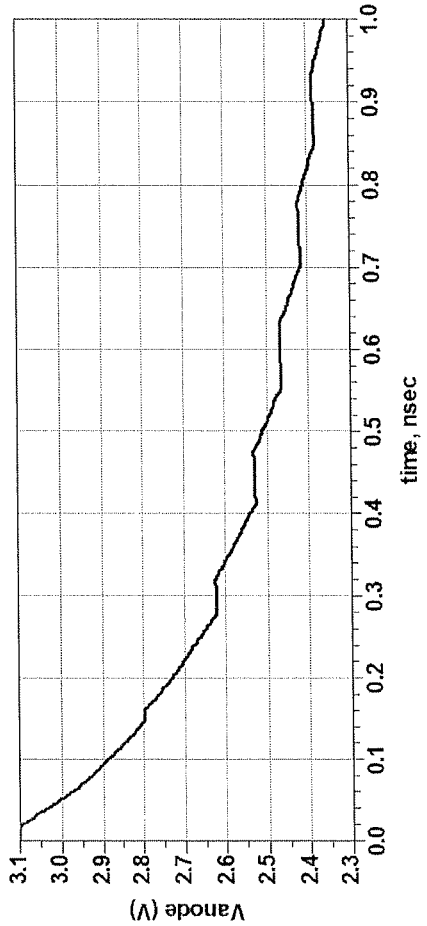


FIG. 15C

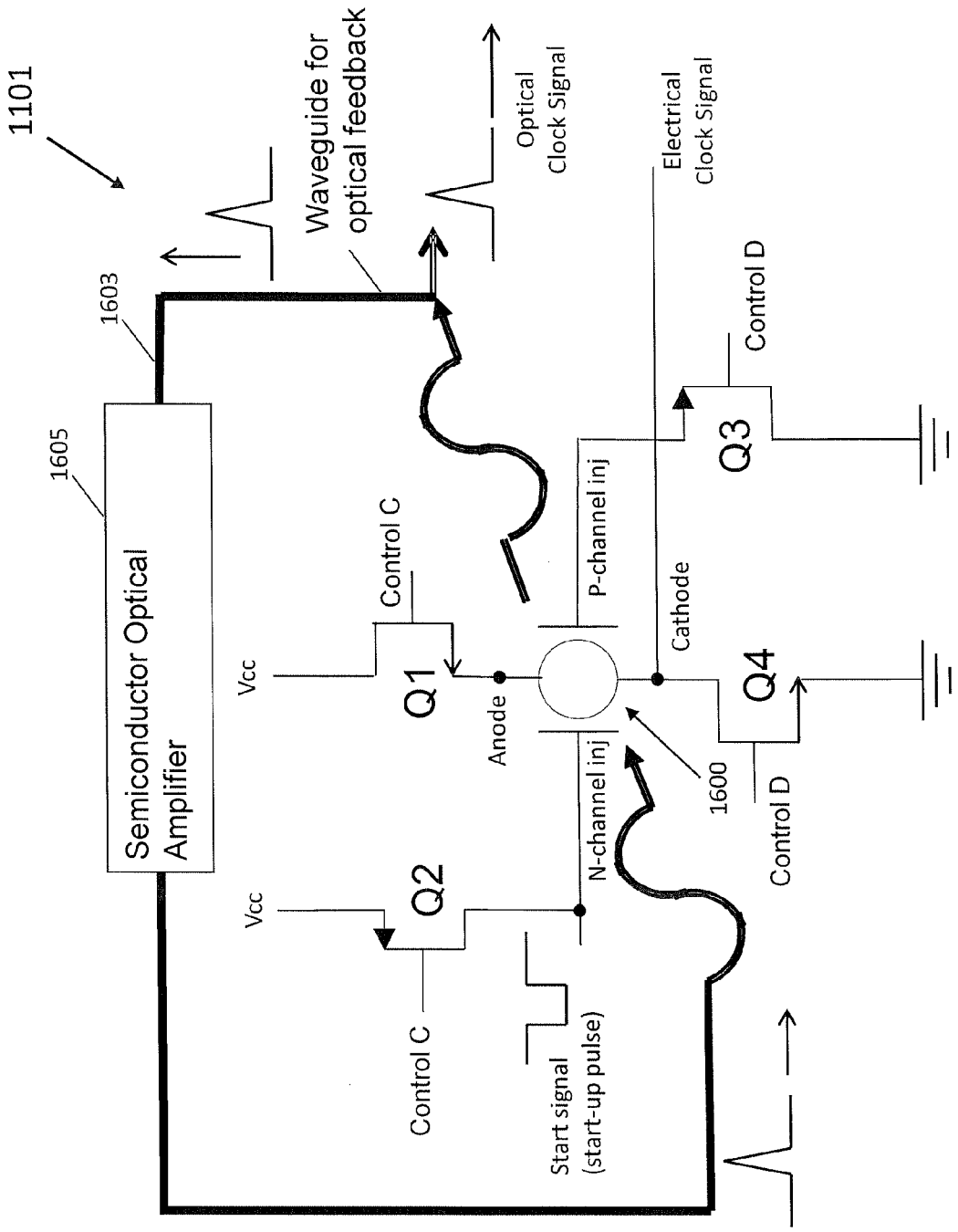

1101
Waveguide for optical feedback
Optical Clock Signal
Electrical Clock Signal
1603
1605
Semiconductor Optical Amplifier
Control C
Control D
Q1
Q2
Q3
Q4
Vcc
Vcc
Anode
Cathode
P-channel inj
N-channel inj
1600
Control C
Control D
Start signal (start-up pulse)

FIG. 16

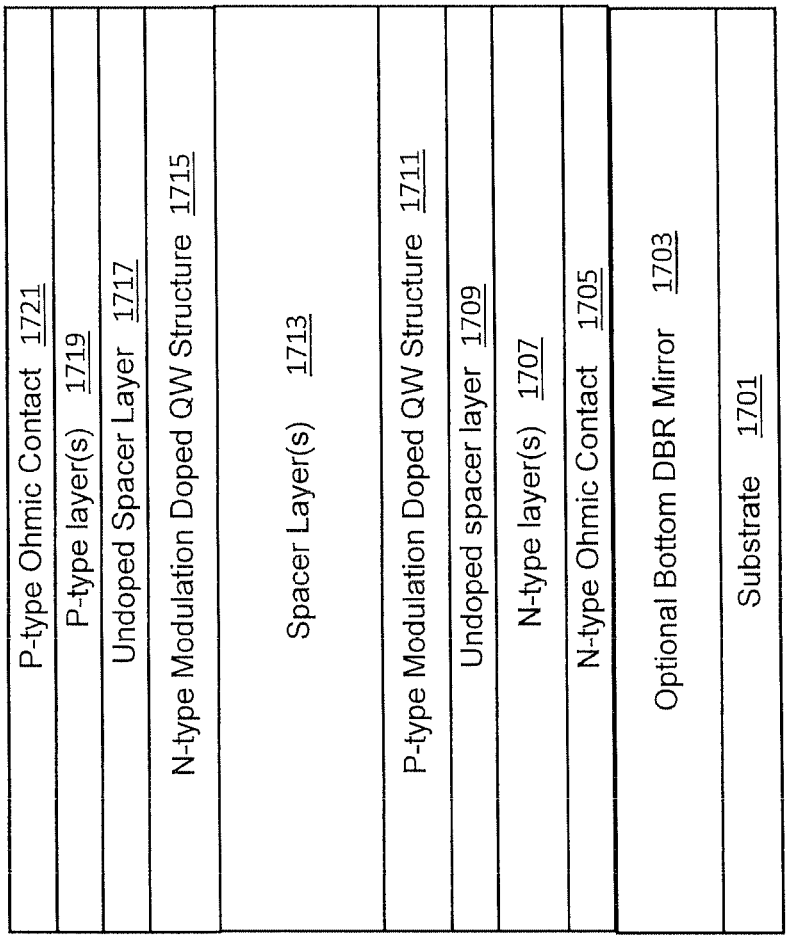

P-type Ohmic Contact 1721
P-type layer(s) 1719
Undoped Spacer Layer 1717
N-type Modulation Doped QW Structure 1715
Spacer Layer(s) 1713
P-type Modulation Doped QW Structure 1711
Undoped spacer layer 1709
N-type layer(s) 1707
N-type Ohmic Contact 1705
Optional Bottom DBR Mirror 1703
Substrate 1701

FIG. 17

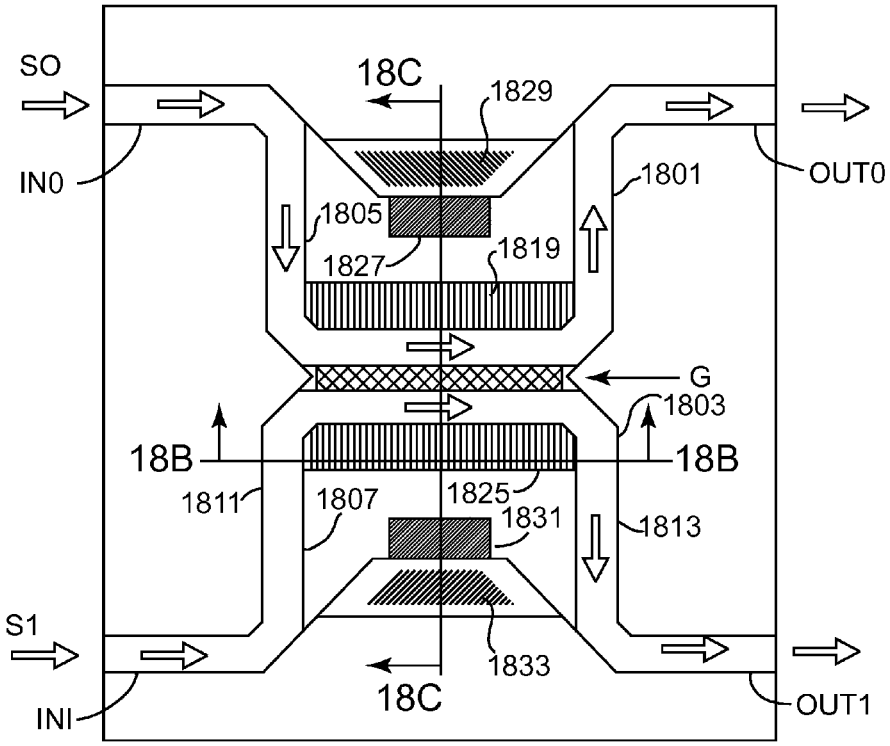

SO
18C
1829
IN0
1801
OUT0
1805
1827
1819
G
1803
18B
18B
1811
1807
1825
1831
1813
S1
1833
18C
INI
OUT1

FIG. 18A

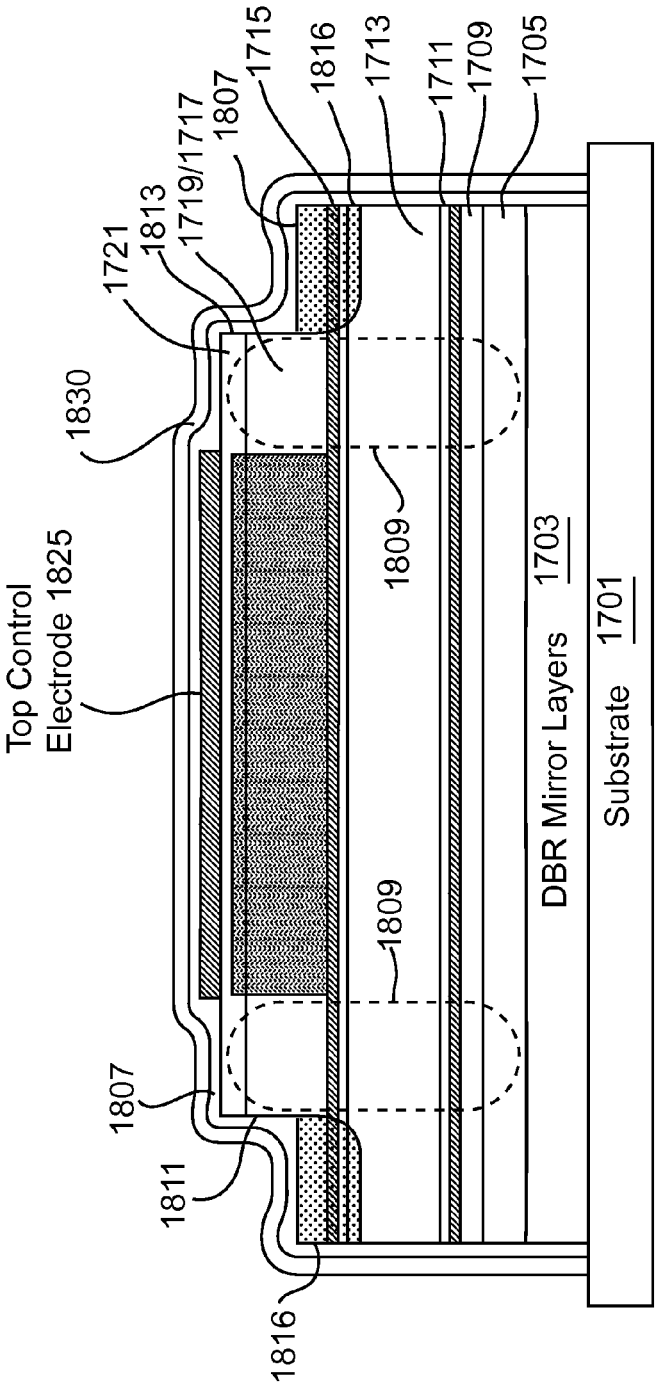

1715
1816
1713
1711
1709
1705
1807
1719/1717
1813
1721
1830
Top Control Electrode 1825
1809
1809
1807
1811
1816
DBR Mirror Layers 1703
Substrate 1701

FIG. 18B

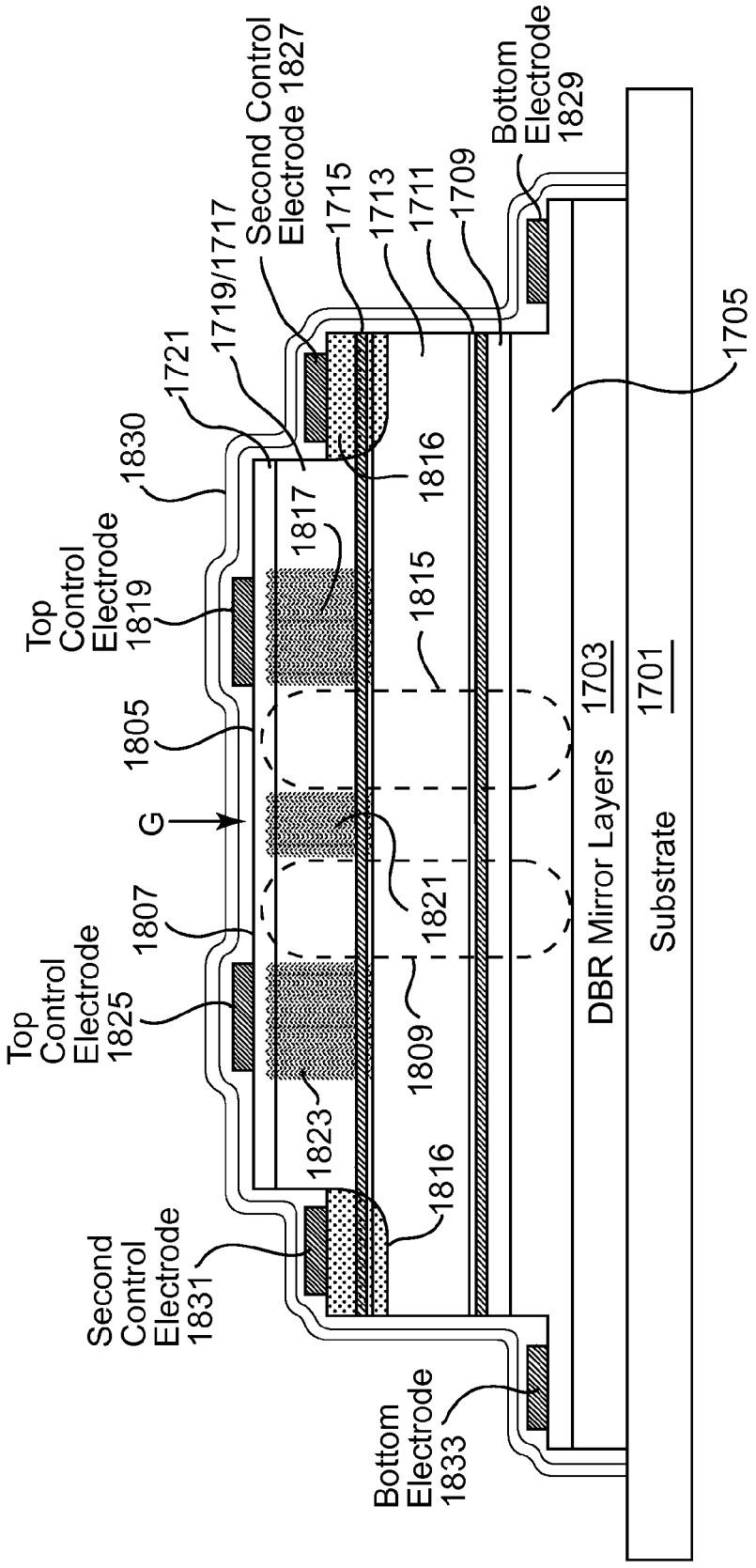

Second Control Electrode 1827
Bottom Electrode 1829
1719/1717
1721
1830
1715
1713
1711
1709
1705
Top Control Electrode 1819
1817
1816
1815
1805
G
1807
Top Control Electrode 1825
1821
1809
1823
1816
Second Control Electrode 1831
Bottom Electrode 1833
DBR Mirror Layers 1703
Substrate 1701

FIG. 18C

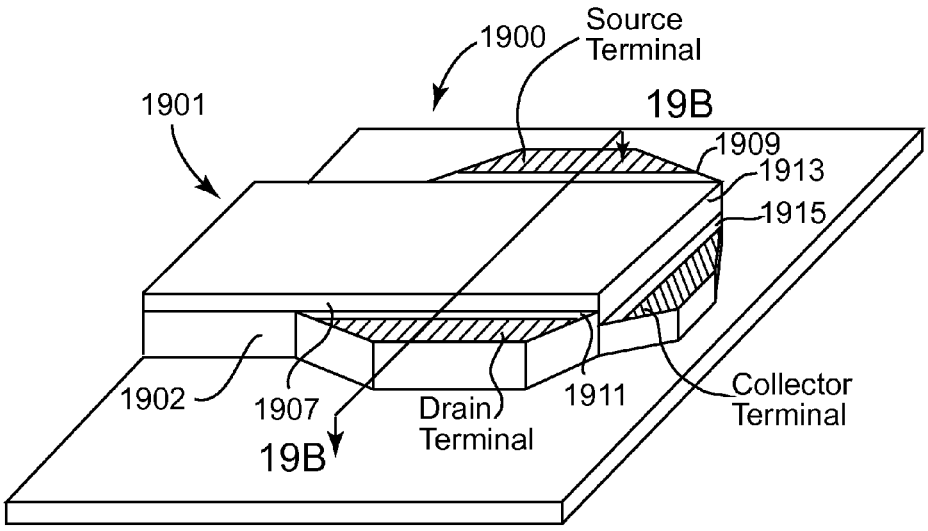


FIG. 19A

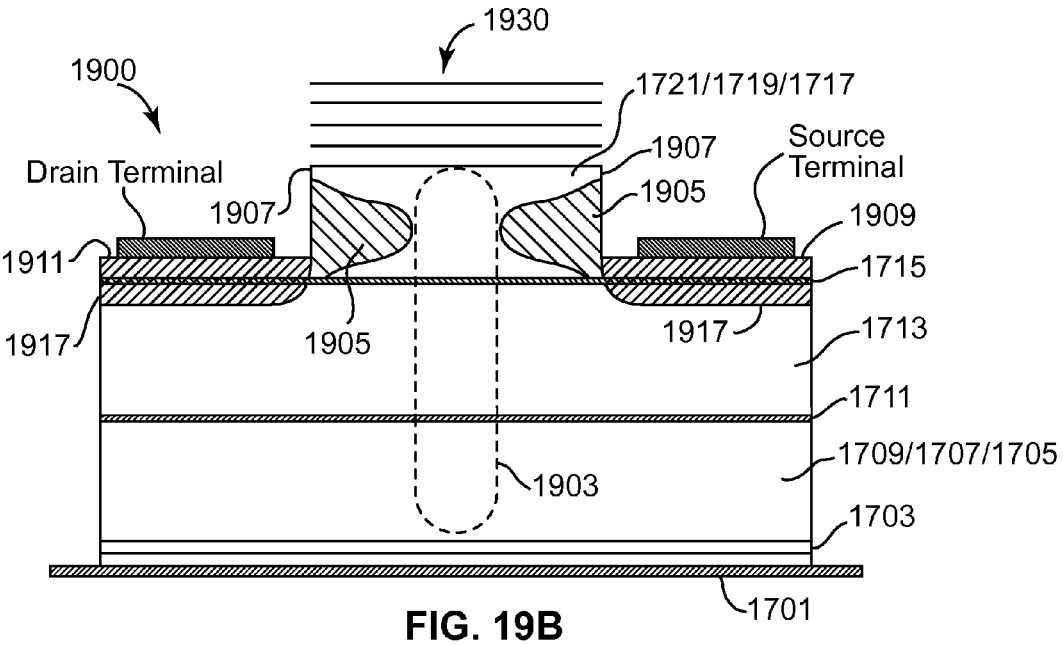


FIG. 19B

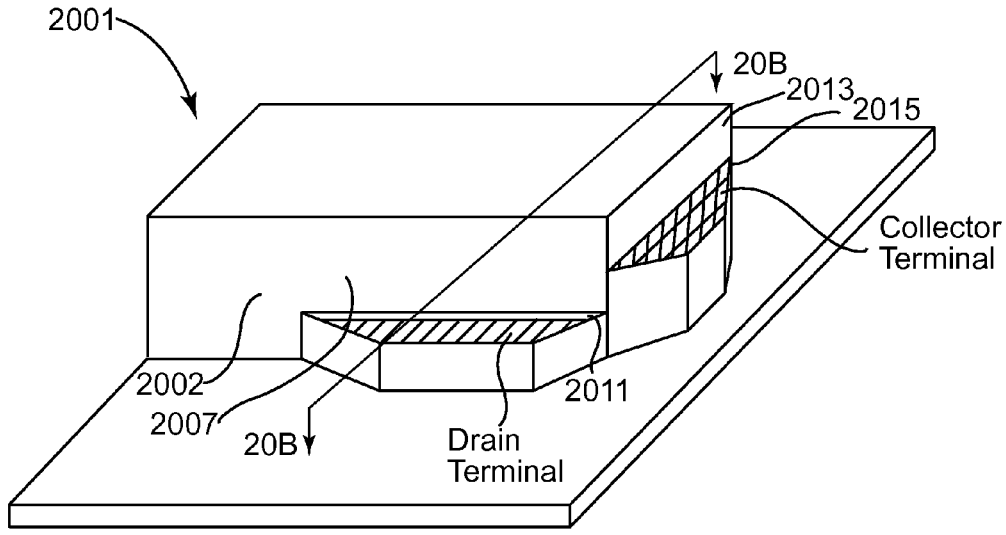


FIG. 20A

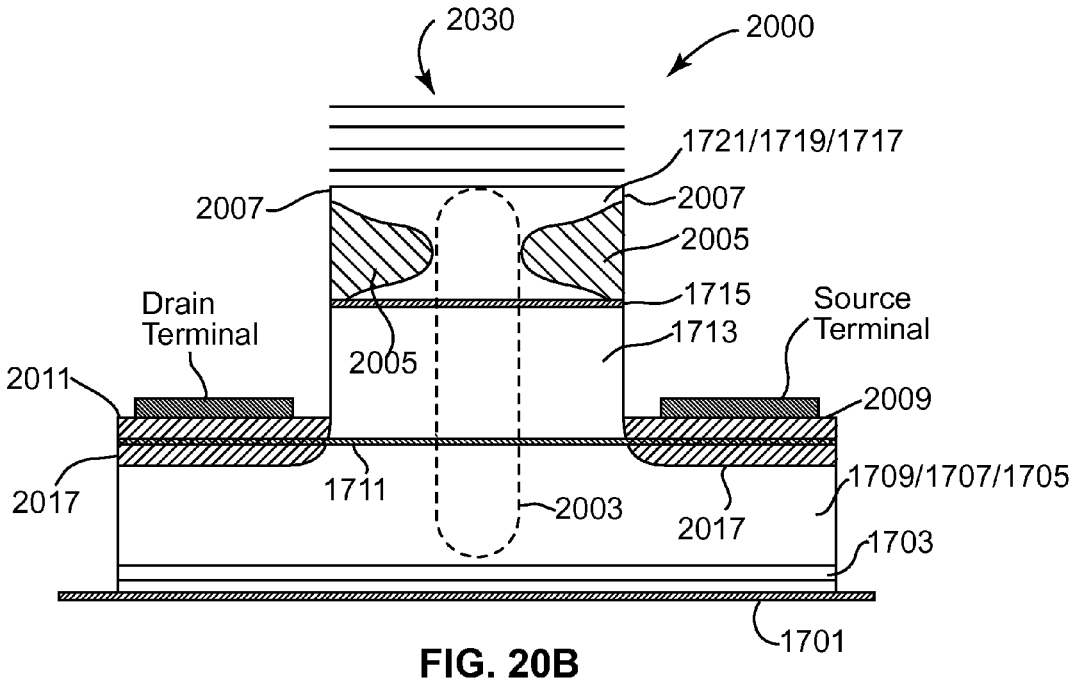


FIG. 20B

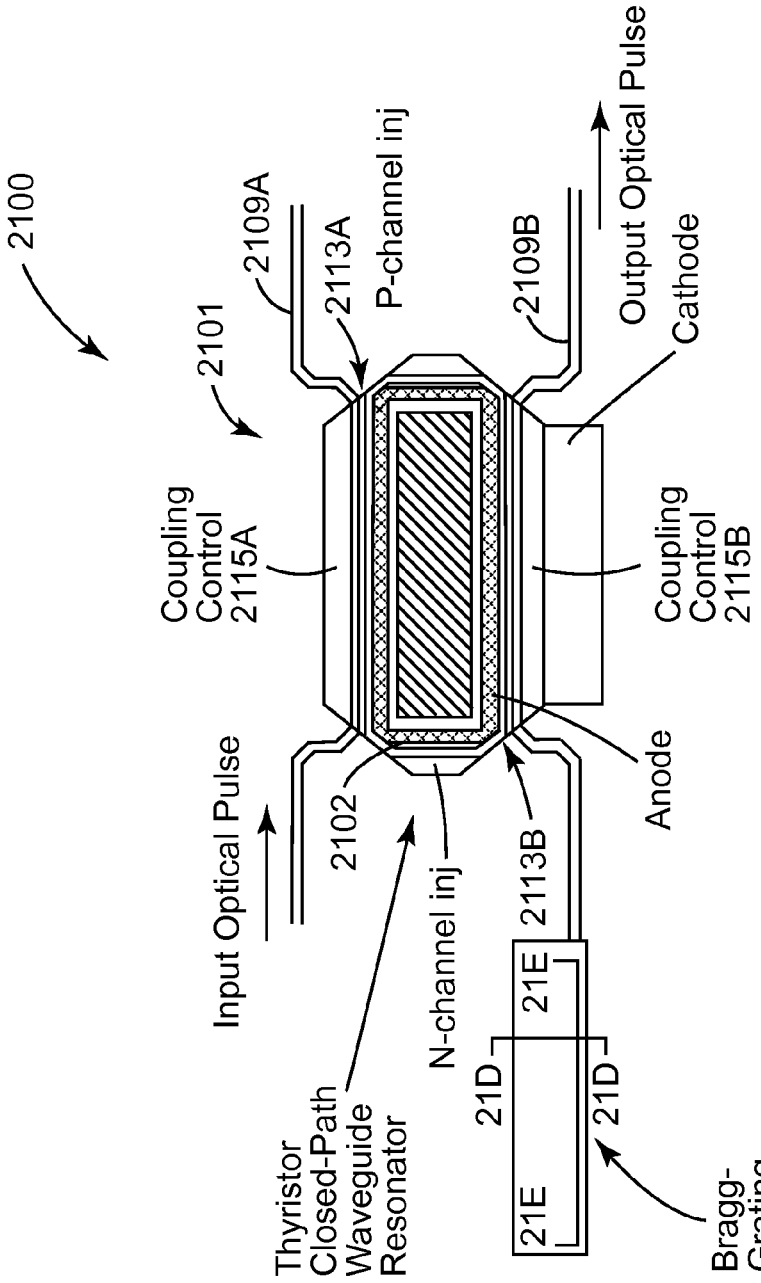

2100
2101
2109A
2113A
P-channel inj
2109B
Output Optical Pulse
Cathode
Coupling Control 2115A
Coupling Control 2115B
Anode
Input Optical Pulse
2102
N-channel inj
2113B
21D
21E
21E
21D
Thyristor Closed-Path Waveguide Resonator
Bragg-Grating Reflector 2121

FIG. 21A

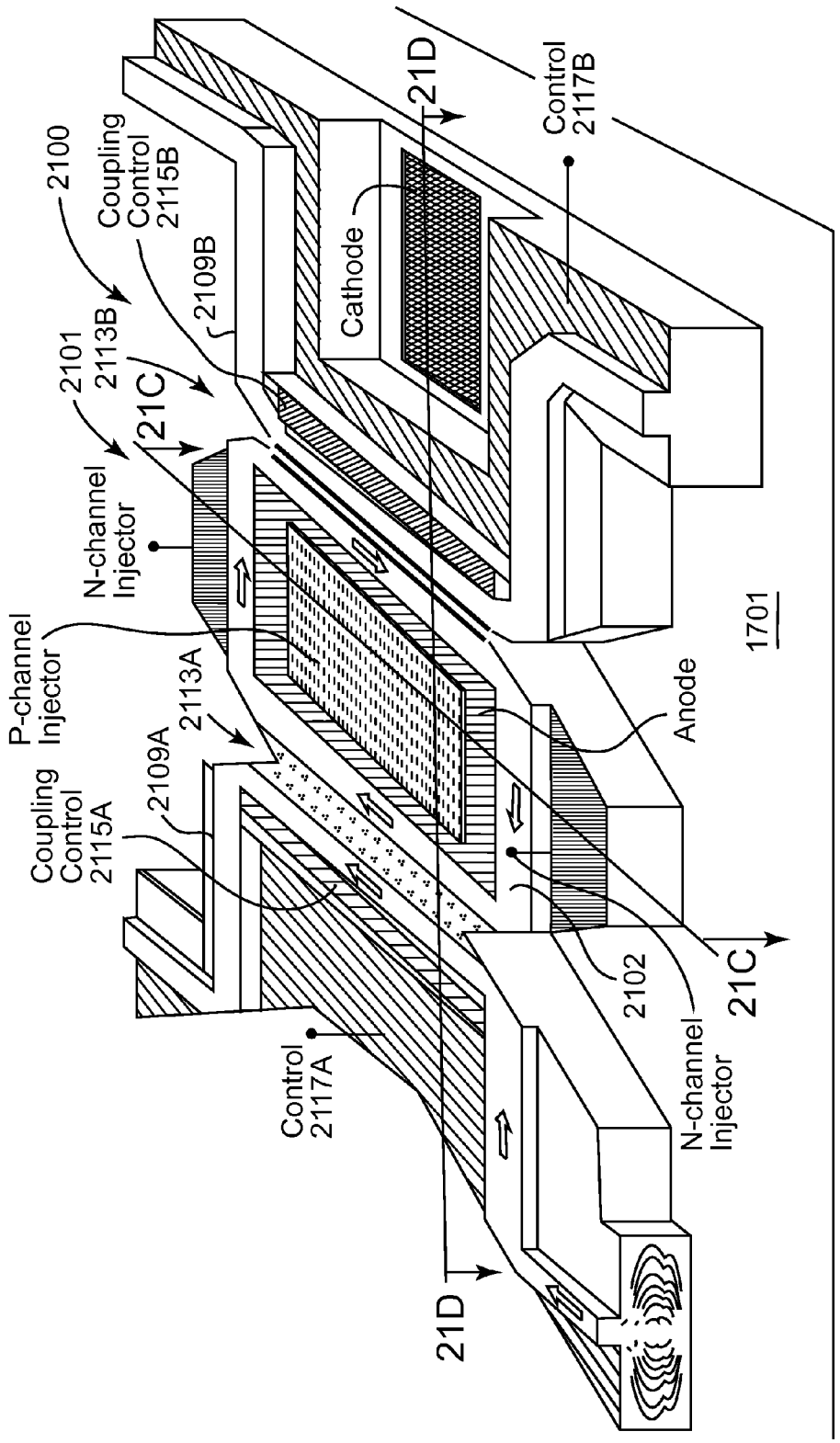

2100
Coupling Control 2115B
2109B
Cathode
21D
Control 2117B
2101
2113B
21C
N-channel Injector
P-channel Injector
2113A
2109A
Coupling Control 2115A
Anode
1701
Control 2117A
2102
21C
N-channel Injector
21D

FIG. 21B

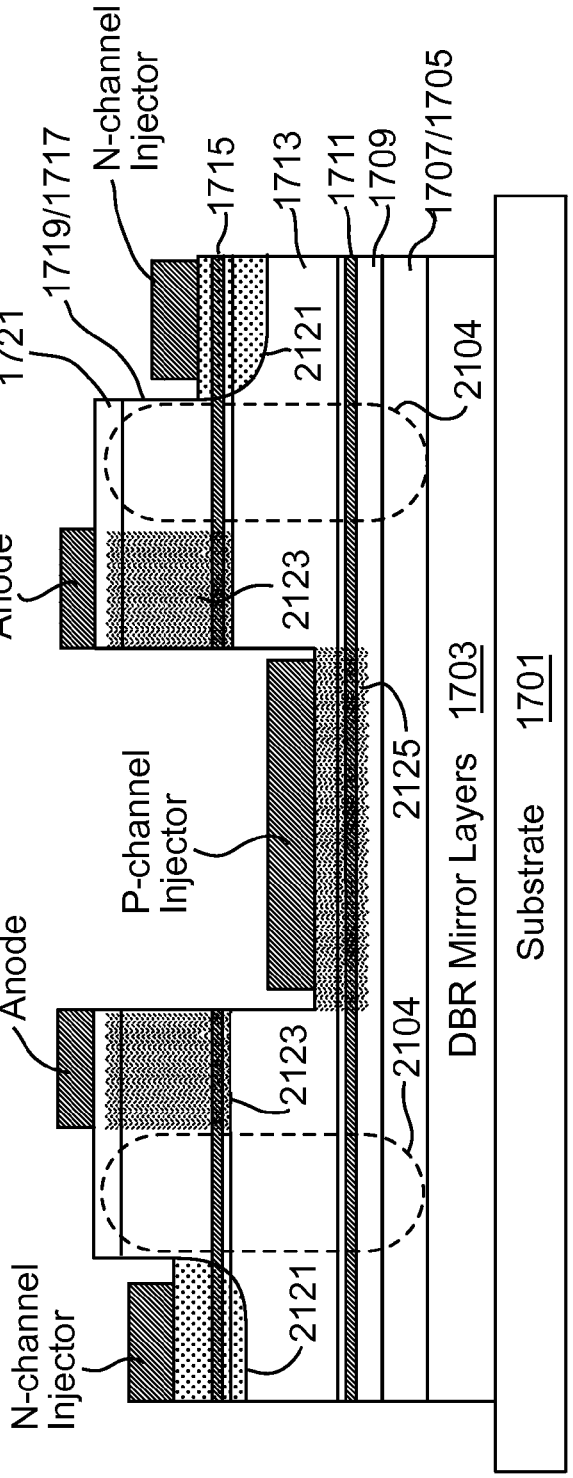

N-channel Injector
1719/1717
1721
Anode
P-channel Injector
Anode
N-channel Injector
1715
1713
1711
1709
1707/1705
2121
2123
2125
2104
2123
2104
2121
DBR Mirror Layers 1703
Substrate 1701

FIG. 21C

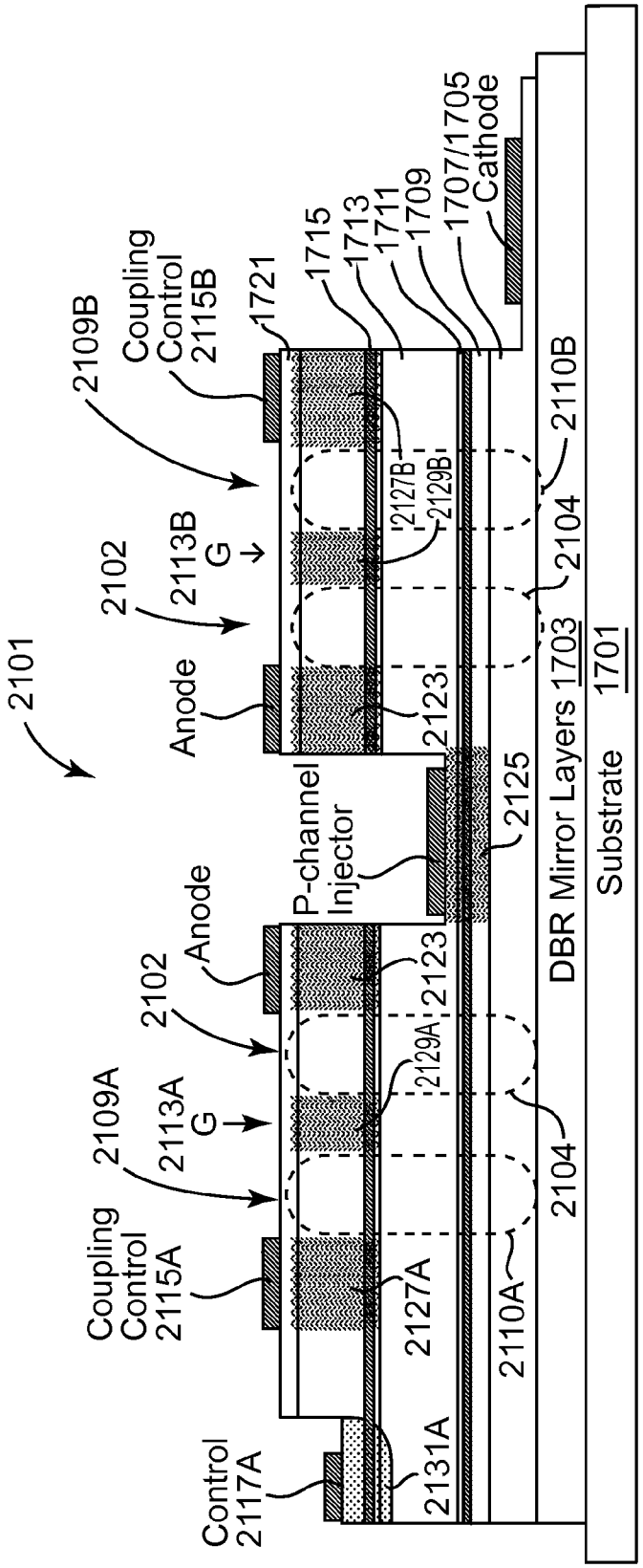

2101
2102
2109B
Coupling Control 2115B
2113B
G
1721
1715
1713
1711
1709
1707/1705 Cathode
Anode
2123
2127B
2129B
2110B
2104
P-channel Injector
2125
DBR Mirror Layers 1703
Substrate 1701
2102
Anode
2123
2109A
2113A
G
2129A
Coupling Control 2115A
2127A
2104
2110A
Control 2117A
2131A

FIG. 21D

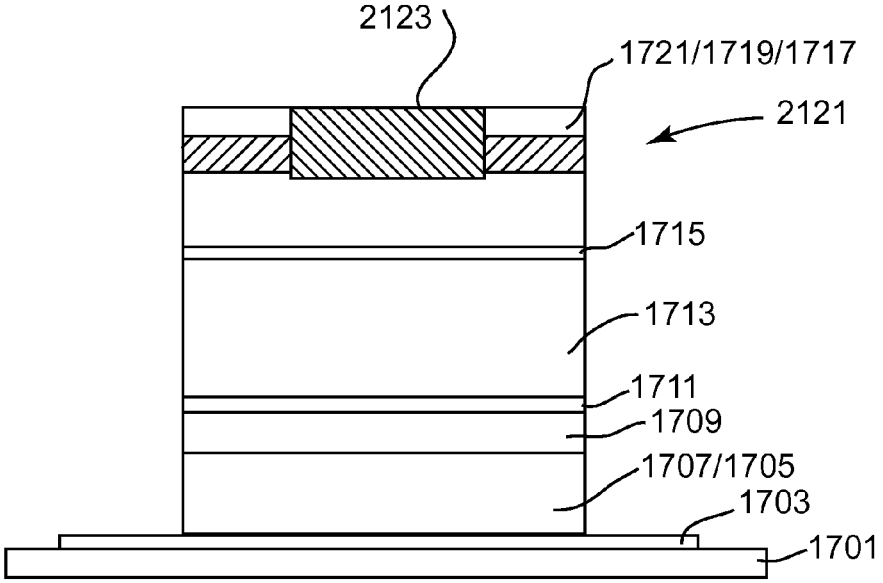

2123
1721/1719/1717
2121
1715
1713
1711
1709
1707/1705
1703
1701

FIG. 21E

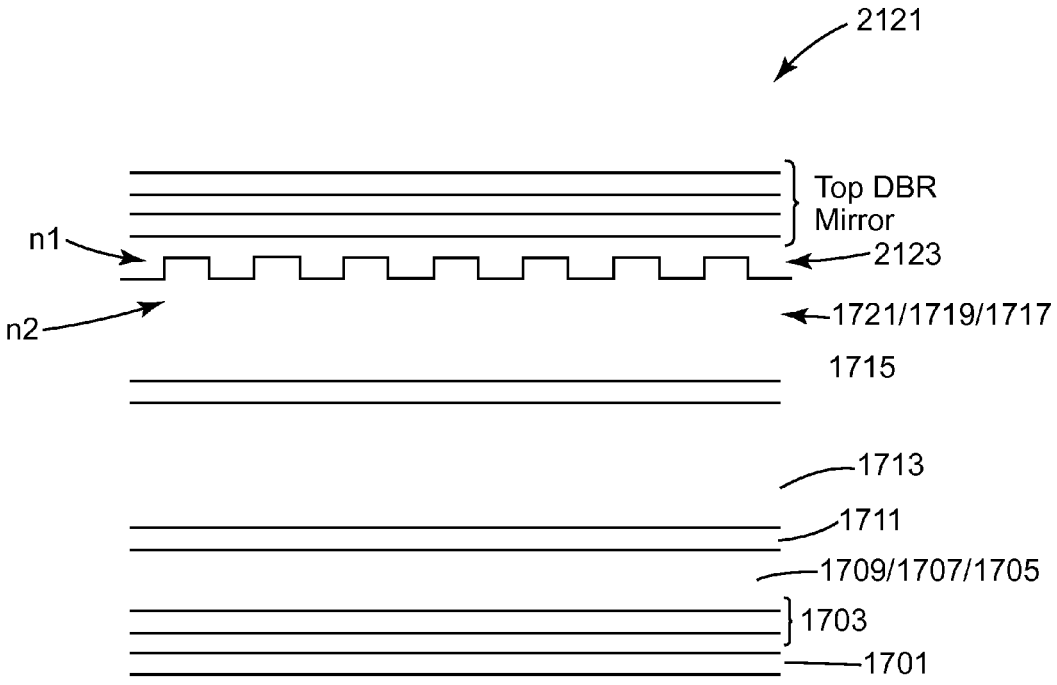

2121
Top DBR
Mirror
n1
2123
n2
1721/1719/1717
1715
1713
1711
1709/1707/1705
1703
1701

FIG. 21F

THYRISTOR-BASED OPTICAL CHARGE PUMP FOR AN OPTICAL PHASE LOCK LOOP

BACKGROUND

1. Field

The present disclosure relates to optical communication systems and, in particular, to receivers of optical communication signals as well as optical and electro-optical components thereof.

2. State of the Art

Phase-shift keying (PSK) is a digital modulation scheme used in optical communication that conveys data by changing, or modulating, the phase of a reference optical signal (the optical carrier wave). PSK uses a finite number of phases, each assigned a unique pattern of binary digits. Usually, each phase encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase. The demodulator (or receiver), which is designed specifically for the symbol-set used by the modulator (or transmitter), determines the phase of the received optical signal and maps it back to the symbol it represents, thus recovering the original data. One form of demodulation requires that the receiver be able to compare the phase of the received optical signal to an optical local oscillating signal whose phase tracks the phase of the reference optical signal. Such a receiver is commonly referred to as a coherent PSK optical receiver. The coherent PSK optical receiver typically employs an optical phase lock loop to synchronize the phase of the optical local oscillating signal to the phase of the reference optical signal used by the transmitter.

Constellation diagrams are commonly used to represent PSK schemes. The constellation diagram shows points in the complex plane where, in this context, the real and imaginary axes are termed the in-phase and quadrature axes respectively due to their 90° separation. Such a representation on perpendicular axes lends itself to straightforward implementation. Specifically, the constellation points are typically selected with uniform angular spacing around a circle. This gives maximum phase-separation between adjacent points and thus the best immunity to corruption. They are positioned on a circle so that they can all be transmitted with the same energy. In this way, the moduli of the complex numbers they represent will be the same and the amplitude of the phase-modulated carrier wave does not change.

Two common PSK schemes are binary phase-shift keying (BPSK or 2-PSK) which uses two phases separated by 180 degrees, and quadrature phase-shift keying (QPSK or 4-PSK) or which uses four phases separated by 90 degrees, although any number of phases may be used. Since the data to be conveyed are usually binary (or digital) in nature, the PSK scheme is usually designed with the number of constellation points being a power of 2. The higher-order PSK schemes are typically labeled with the number of phases used for the respective scheme. Thus, a PSK scheme employing 8 phases separated by 45 degrees is commonly referred to as 8-PSK, a PSK scheme employing 16 phases separated by 22.5 degrees is commonly referred to 16-PSK, and a generic PSK employing M phases separated by (360/M) degrees is commonly referred to as M-PSK or M-ary PSK.

For the coherent BPSK optical receiver, the phase-aligned local oscillating signal can be split and mixed in the optical domain by a network of 3-dB fiber couplers for supply to corresponding photodetectors as shown in FIG. **1**. This configuration converts the received optical signal to baseband electrical signals that represents the in-phase component and quadrature component of the received optical signal. These two component signals can be processed in the electrical domain by a signal processor in order to determine the phase of the received optical signal and map it back to the symbol it represents, thus recovering the original data.

SUMMARY

The present disclosure relates to a charge pump circuit suitable for use in an optical phase lock loop. The charge pump circuit includes first and second optical thyristors, wherein the first optical thyristor is configured to receive a first digital optical signal input, and wherein the second optical thyristor is configured to receive a second digital optical signal input. A first filter circuit operably coupled to the first optical thyristor. First control circuitry is operably coupled to terminals of the first optical thyristor and receives a first digital electrical signal input corresponding to the second digital optical signal input. A second filter circuit is operably coupled to said second optical thyristor. Second control circuitry is operably coupled to terminals of said second optical thyristor and receives a second digital electrical signal input corresponding to the first digital optical signal input. The first control circuitry is configured to control switching operation of the first optical thyristor that sources current to the first filter circuit in response to the levels of the first digital optical signal input and the first digital electrical signal input. The second control circuitry is configured to control switching operation of the second optical thyristor that sinks current from the second filter circuit in response to the levels of the second digital optical signal input and the second digital electrical signal input.

In one embodiment, the first filter circuit can be configured to perform integration of increases in voltage potential of a cathode terminal of the first optical thyristor over time, and the second filter circuit can be configured to perform integration of decreases in voltage potential of an anode terminal of the second optical thyristor over time. The result of the integration performed by the first filter circuit van be an increasing voltage signal at the cathode terminal of the first optical thyristor whose change over time tracks the phase offset of the first digital optical signal input and the second digital optical input. The result of the integration performed by the second filter circuit can be a decreasing voltage signal at the anode terminal of the second optical thyristor whose change over time tracks the phase offset of the second digital optical signal input and the first digital optical input.

In one embodiment, the first and second optical thyristors can each be defined by an epitaxial layer structure that includes a bottom n-type cathode region, an intermediate p-type region formed above the bottom n-type region, an intermediate n-type region formed above the intermediate p-type region, and a top p-type anode region formed above the intermediate n-type region. Furthermore, each optical thyristor can include an anode terminal electrically coupled to the top p-type anode region, an n-type injector terminal electrically coupled to the intermediate n-type region, a p-type injector terminal electrically coupled to the intermediate p-type region, and a cathode terminal electrically coupled to the n-type cathode region.

In one embodiment, the first control circuit can include a first field-effect transistor whose source-drain current path is electrically coupled between a positive voltage supply and the n-type injector terminal of said first optical thyristor. The first digital electrical signal input corresponding to the second digital optical signal input can be supplied to the first field-effect transistor in order to control switching operation of the

first optical thyristor. The first field-effect transistor can be an n-channel HFET transistor having a gate terminal that receives the first digital electrical signal input corresponding to the second digital optical signal input. The first control circuit can include a second field-effect transistor whose source-drain current path is electrically coupled between a negative or ground power supply and the p-type injector terminal of the first optical thyristor. The first digital electrical signal input corresponding to the second digital optical signal input can be supplied to the second field-effect transistor in order to control switching operation of said first optical thyristor. The second field-effect transistor can be an n-channel HFET transistor having a gate terminal that receives the first digital electrical signal input corresponding to the second digital optical signal input.

In one embodiment, the second control circuit can include a third field-effect transistor whose source-drain current path is electrically coupled between a positive voltage supply and the n-type injector terminal of the second optical thyristor. The second digital electrical signal input corresponding to the first digital optical signal input can be supplied to said third field-effect transistor in order to control switching operation of the second optical thyristor. The third field-effect transistor can be an n-channel HFET transistor having a gate terminal that receives the second digital electrical signal input corresponding to the first digital optical signal input. The second control circuit can include a fourth field-effect transistor whose source-drain current path is electrically coupled between a negative or ground power supply and the p-type injector terminal of the second optical thyristor. The second digital electrical signal input corresponding to the first digital optical signal input can be supplied to the fourth field-effect transistor in order to control switching operation of the second optical thyristor. The fourth field-effect transistor can be an n-channel HFET transistor having a gate terminal that receives the second digital electrical signal input corresponding to the first digital optical signal input.

In one embodiment, the intermediate n-type and p-type regions of the epitaxial layer structure of the optical thyristor can include an n-type modulation doped QW structure and a p-type modulation doped QW structure, respectively. The first and second control circuits can include at last one field effect transistor that includes an n-type QW channel formed by the n-type modulation doped QW structure of the epitaxial layer structure of the first and second optical thyristors and/or a p-type QW channel formed by the n-type modulation doped QW structure of the epitaxial layer structure of the first and second optical thyristors. The epitaxial layer structure of the first and second optical thyristors can be formed from group III-V materials.

In another aspect, the present disclosure relates to an optical phase lock loop that includes an optical clock source, an optical phase detector and a feedback circuit. The optical clock source generates an optical clock signal. The optical phase detector measures phase difference between a reference optical signal and the optical clock signal generated by the optical clock source. The feedback circuit is configured to generate first and second control signal inputs for supply to the optical clock source. The feedback circuit can include a charge pump circuit as described herein. The optical clock source can include another optical thyristor. The optical phase detector can include an optical flip-flop realized by another optical thyristor. The optical phase detector can include an optical AND gate realized by another optical thyristor and/or an AND gate realized by a thyristor. In one embodiment, the optical phase lock loop can be configured to perform a clock recovery function.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a prior art coherent BPSK optical receiver.

FIG. **2**A is a schematic block diagram of coherent BPSK optical communication system that can embody aspects of the present disclosure.

FIG. **2**B is a schematic block diagram of an illustrative embodiment of coherent BPSK optical receiver according to the present disclosure.

FIG. **3**A is a schematic circuit diagram of the optical mixer and thyristor-based optical BPSK detector of FIG. **2**B.

FIG. **3**B is a table of an exemplary mapping of phases to binary symbols represented by the digital output signal produced by the optical BPSK detector of FIG. **3**A.

FIG. **3**C is a constellation diagram of the exemplary mapping of phases to binary symbols as shown in the table of FIG. **3**B.

FIG. **4** is a schematic block diagram of coherent PSK optical communication system that can embody aspects of the present disclosure.

FIG. **5** is a schematic block diagram of an illustrative embodiment of coherent PSK optical receiver according to the present disclosure.

FIG. **6**A is a schematic diagram of an optical mixer and thyristor-based optical QPSK detector, suitable for use in the coherent PSK optical receiver of FIG. **5** that receives optical QPSK-modulated signals.

FIG. **6**B is a table of an exemplary mapping of phases to four symbols represented by the digital output signals produced by the optical QPSK detector of FIG. **6**A.

FIG. **6**C is a constellation diagram of the exemplary mapping of phases to symbols as shown in the table of FIG. **6**B.

FIG. **7**A is a schematic diagram of an optical mixer and thyristor-based optical 8-PSK detector, suitable for use in the coherent PSK optical receiver of FIG. **5** that receives optical 8-PSK-modulated signals.

FIG. **7**B is a table of an exemplary mapping of phases to eight symbols represented by the digital output signals produced by the optical 8-PSK detector of FIG. **7**A.

FIG. **7**C is a constellation diagram of the exemplary mapping of phases to symbols as shown in the table of FIG. **7**B.

FIG. **8**A is a schematic circuit diagram of a thyristor-based optical XOR circuit according to the present disclosure.

FIG. **8**B is a table showing the XOR function provided by the optical XOR circuit of FIG. **8**A.

FIGS. **9**A and **9**B, collectively, is a schematic diagram of the optical mixer and thyristor-based optical 16-PSK detector, suitable for use in the coherent PSK optical receiver of FIG. **5** that receives optical 16-PSK-modulated signals.

FIG. **9**C is a table of an exemplary mapping of phases to sixteen symbols represented by the digital output signals produced by the optical 16-PSK detector of FIGS. **9**A and **9**B.

FIG. **9**D is a constellation diagram of the exemplary mapping of phases to symbols as shown in the table of FIG. **9**C.

FIGS. **10**A and **10**B, collectively, is a schematic diagram of the optical mixer and thyristor-based optical PSK-QAM detector, suitable for use in the coherent PSK optical receiver of FIG. **5** that receives optical PSK-QAM-modulated signals.

FIG. **10**C is a table of an exemplary mapping of phases and two amplitude modulations (T**1** and T**2**) to eight symbols represented by the digital output signals produced by the optical PSK-QAM detector of FIGS. **10**A and **10**B.

FIG. **10**D is a constellation diagram of the exemplary mapping of phases and two amplitude modulations (T**1** and T**2**) to eight symbols as shown in the table of FIG. **10**C.

FIG. **10**E is a schematic circuit diagram of part of the optical PSK-QAM detector of FIGS. **10**A and **10**B for detecting the phases of the T**2** amplitude modulation level.

FIG. **10**F is a table of an exemplary mapping of phases and two amplitude modulations (T**3** and T**4**) to eight symbols represented by the digital output signals produced by the optical PSK-QAM detector of FIGS. **10**A and **10**B.

FIG. **10**G is a constellation diagram of the exemplary mapping of phases and two amplitude modulations (T**3** and T**4**) to eight symbols as shown in the table of FIG. **10**F.

FIG. **10**H is a schematic circuit diagram of part of the optical PSK-QAM detector of FIGS. **10**A and **10**B for detecting the phases of the T**3** amplitude modulation level.

FIG. **10**I is a schematic circuit diagram of part of the optical PSK-QAM detector of FIGS. **10**A and **10**B for detecting the phases of the T**4** amplitude modulation level.

FIG. **10**J shows the full constellation diagram of the exemplary mapping of phases and four amplitude modulations (T**1**, T**2**, T**3** and T**4**) to sixteen symbols that can be detected by the optical PSK-QAM detector of FIGS. **10**A and **10**B.

FIG. **11** is a schematic block diagram of an exemplary embodiment of the optical phase lock loop (OPPL) that functions as clock recovery circuit suitable for use in the coherent optical receivers of FIGS. **2**A and **5**.

FIG. **12**A is a schematic diagram of an exemplary embodiment of optical phase detector suitable for use in the optical phase lock loop (clock recovery circuit) of FIG. **11**.

FIG. **12**B is a table illustrating the logic function of the optical flip-flop A of FIG. **12**A.

FIG. **12**C is a table illustrating the logic function of the optical flip-flop B of FIG. **12**A.

FIG. **12**D is a table illustrating the logic function of the AND gate of FIG. **12**A.

FIG. **13**A is a schematic circuit diagram of an exemplary embodiment of an optical flip-flop, which is configured for use as the optical flip-flop A of FIG. **12**A.

FIG. **13**B is a schematic circuit diagram of an exemplary embodiment of an optical flip flop, which is configured for use as the optical flip-flop B of FIG. **12**A.

FIG. **14**A is a schematic circuit diagram of an exemplary embodiment of an AND gate, which is configured for use as the AND gate of FIG. **12**A.

FIG. **14**B is a schematic circuit diagram of an exemplary embodiment of an optical AND gate, which is configured for use as the AND gate of FIG. **12**A.

FIG. **15**A is a schematic diagram of an exemplary embodiment of optical charge pump and loop filter circuit suitable for use in the optical phase lock loop (clock recovery circuit) of FIG. **11**.

FIG. **15**B is a graph illustrating an example of a control signal D generated by the optical charge pump and loop filter circuit of FIG. **15**A.

FIG. **15**C is a graph illustrating an example of a control signal C generated by the optical charge pump and loop filter circuit of FIG. **15**A.

FIG. **16** is a schematic diagram of an exemplary embodiment of optoelectronic oscillator suitable for use in the optical phase lock loop (clock recovery circuit) of FIG. **11**.

FIG. **17** is a schematic illustration of an exemplary epitaxial layer structure that can be used to realize the electrical devices, optoelectronic devices and optical devices of the various circuit arrangements described herein.

FIGS. **18**A-**18**C are schematic illustrations of an exemplary embodiment of an optical hybrid coupler that can be made utilizing the layer structure of FIG. **17**.

FIGS. **19**A and **19**B are schematic illustrations of an exemplary embodiment of an n-channel HFET phototransistor device that can be made utilizing the layer structure of FIG. **17**.

FIGS. **20**A and **20**B are schematic illustrations of an exemplary embodiment of a p-channel HFET phototransistor device that can be made utilizing the layer structure of FIG. **17**.

FIGS. **21**A-**21**F are schematic illustrations of an exemplary embodiment of an optical thyristor and associated optoelectronic circuit elements that can be made utilizing the layer structure of FIG. **17** and configured for use as an optoelectronic oscillator.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **2**A shows an optical communication system **100** employing optical binary phase shift keying (BPSK) signals. The system **100** includes a transmitter **112** having a laser local oscillator **114** that generates an optical carrier signal at a predetermined wavelength. The intensity of the optical carrier signal output by the laser local oscillator **114** oscillates at a predefined frequency. The laser local oscillator **114** can be a distributed feedback (DFB) laser or other suitable laser emitter. The optical carrier signal output by the laser local oscillator **114** is supplied to an optical BPSK modulator **116** that modulates the phase of the optical carrier signal according to a supplied signal stream of binary bit values and a symbol clock. The symbol clock defines the timing of the boundaries for the individual bit values of the signal stream. For a binary bit value of "1" in the signal stream, the optical BPSK modulator **116** produces a phase-shifted optical carrier signal that has a predefined corresponding phase offset (such as 0 degrees phase offset) relative to the carrier optical signal output by the laser local oscillator **114**. For a binary bit value of "0" in the signal stream, the optical BPSK modulator **116** produces a phase-shifted optical carrier signal that has a predefined corresponding phase offset (such as a 180 degree or π phase offset) relative to the carrier optical signal output by the laser local oscillator **114**. The optical BPSK modulator **116** can function to incorporate time delay into the optical signal path corresponding to the required phase change (as $\Delta\phi=\omega\Delta t$). This can be realized by a ring resonator where the effective optical velocity through the ring resonator is controlled in some manner (such as in response to one or more electrical signals supplied to the ring resonator). The phase-shifted optical carrier signal produced by the optical BPSK modulator **116** is carried by a communication medium **118** (such as an optical fiber) to a receiver **120**.

The receiver **120** receives the phase-shifted optical carrier signal carried over the communication medium **118**. The receiver **120** includes a laser local oscillator that is part of an optical phase lock loop (OPPL) **122** that functions to recover the optical carrier signal from the received optical phase-shifted carrier signal. In this manner, the laser local oscillator of the OPPL **122** of the receiver **120** generates an optical signal (referred to as an "optical local oscillating signal") that oscillates at a frequency and phase that matches the optical carrier signal output by the laser local oscillator **114** of the transmitter **112**. The OPPL **122** estimates and compensates for differences in oscillation frequency between the receiver's laser local oscillator and the optical carrier signal of the transmitter **112**. It also aligns the phase of the receiver's laser local oscillator to the phase of the optical carrier signal of the transmitter **112**. The optical local oscillating signal generated by the OPPL **122** along with the received optical phase-

shifted carrier signal are processed by an optical BPSK coherent demodulator **124** to identify the phase offset of the received optical phased-shifted carrier signal relative to the optical local oscillating signal. This is a form of coherent homodyne detection of the phase information carried in the received phased-shifted optical carrier signal. The optical BPSK coherent demodulator **124** generates an electrical signal that encodes the binary bit values corresponding to the phase offset information of the received phased-shifted optical carrier signal. The correspondence between the phase offset information and the binary bit values is dictated by the BPSK modulation scheme employed by the optical BPSK modulator **116** of the transmitter **112**. In this manner, the optical BPSK coherent demodulator **124** recovers the signal stream of binary bit values carried by the received phase-shifted optical carrier signal. The optical BPSK coherent demodulator **124** also operates to generate an electrical clock signal (timing information) corresponding to the symbol clock of the transmitter **112**. The recovered signal stream and the clock signal are supplied to circuitry **126** that decodes the signal stream (if necessary) and performs serial-to-parallel data conversion. The parallel data (typically, byte-sizes chunks) can be output to a data processing circuit as needed.

FIG. **2**B is a block diagram illustrating an embodiment of the receiver **120** of FIG. **2**A, which includes an OPPL **122**, an optical mixer and thyristor-based optical BPSK detector **124**A, an optical clock recover block **124**B, and signal decode circuitry **126**. The OPPL **122** includes a laser local oscillator **201** and a loop filter **203**. The loop filter **203** functions to estimate and compensate for differences in oscillation frequency between the optical local oscillating signal generated by the laser local oscillator **201** and the optical carrier signal of the transmitter **112**. The loop filter **203** also functions to align the phase of the optical local oscillating signal to the phase of the optical carrier signal of the transmitter **112**. The output of the laser local oscillator is supplied to a polarization control module **205** that fixes the polarization state of the optical local oscillating signal to match the polarization of the received optical signal. This may be necessary as the laser local oscillator **201** may produce an optical polarization state that differs from the received optical signal.

The optical mixer and thyristor-based optical BPSK detector **124**A is configured to identify the phase offset of the received optical phased-shifted carrier signal relative to the optical local oscillating signal. This is form of coherent homodyne detection of the phase information carried in the received phased-shifted optical carrier signal. The optical mixer and thyristor-based optical BPSK detector **124**A generates an electrical signal that encodes the binary bit values corresponding to the phase offset information of the received phased-shifted optical carrier signal. The correspondence between the phase offset information and the binary bit values is dictated by the BPSK modulation scheme employed by the optical BPSK modulator **116** of the transmitter **112**. In this manner, the optical mixer and thyristor-based optical BPSK detector **124**A recovers the signal stream of binary bit values carried by the received phase-shifted optical carrier signal.

The optical clock recovery block **124**B operates to generate an electrical clock signal whose ON/OFF transitions are synchronized to the symbol clock of the transmitter. This symbol clock is embedded in the optical signal generated by the optical mixer and thyristor-based optical BPSK detector **124**A, which represents the recovered signal stream of binary bit values carried by the received phase-shifted optical carrier signal and detected by the optical mixer and thyristor-based optical BPSK detector **124**A.

The signal decode circuitry **126** utilizes the electrical clock signal (recovered symbol clock) generated by the clock recovery block **124**B to sample the pulses of the electrical signal generated by the optical mixer and thyristor-based optical BPSK detector **124**A. This electrical signal represents the recovered signal stream of binary bit values carried by the received phase-shifted optical carrier signal and detected by the optical mixer and thyristor-based optical BPSK detector **124**A. This sampling is performed at the timing that corresponds recovered symbol clock and thus is aligned to the binary bit values carried by the received phase-shifted optical carrier signal. The signal decode circuitry **126** also performs signal decoding operations that map each recovered phase sample back to the binary symbol it represents and thus recovers the original data.

An embodiment of the optical mixer and thyristor-based optical BPSK detector **124**A is shown in FIG. **3**A. It employs a network of three 180-degree optical hybrid couplers **300**A, **300**B, **300**C for optical mixing of the received phase-shifted carrier signal and the optical local oscillating signal output by the OPPL **122**.

Each 180-degree optical hybrid coupler includes two input waveguides (In0/In1) and two output waveguides (Out0/Out1). The two input waveguides In0, In1 receive two separate input optical signals **S0** and **S1**. The 180-degree optical hybrid coupler mixes the two input optical signals **S0** and **S1** to produce two output signals that propagate out from the Out0 and Out1 waveguides where the power of the two input optical signals **S0**, **S1** is split evenly (50:50 split for each input signal) in each one of two output signals. Specifically, the intensity **I0** of the optical signal propagating out from the output waveguide Out0 is given as:

$$I0=E_{S1}^2\cos^2(\kappa L_{eff})+E_{S0}^2\sin^2(\kappa L_{eff})+E_{S1}E_{S0}\sin(2\kappa L_{eff})\sin\phi \quad (1)$$

where

- E_{S1} is the field amplitude of the input optical signal **S1** supplied to the In1 input waveguide,
- E_{S0} is the field amplitude of the input optical signal **S0** supplied to the In0 input waveguide,
- κ and L_{eff} is the coupling constant and the effective coupling length of the 180-degree optical hybrid coupler, and
- ϕ is the phase difference in the optical signals produced in the Out0 and Out1 output waveguides.

Similarly, the intensity **I1** of the optical signal propagating out from the output waveguide Out2 is given as:

$$I1=E_{S1}^2\sin^2(\kappa L_{eff})+E_{S0}^2\cos^2(\kappa L_{eff})+E_{S1}E_{S0}\sin(2\kappa L_{eff})\sin\phi \quad (1)$$

In the case of the 50:50 split ratio, κL_{eff} is $\pi/4$ and Eqn. (1) and Eqn. (2) becomes:

$$I0=\tfrac{1}{2}E_{S1}^2+\tfrac{1}{2}E_{S0}^2+E_{S1}E_{S0}\sin\phi, \text{ and} \quad (3)$$

$$I1=\tfrac{1}{2}E_{S1}^2+\tfrac{1}{2}E_{S0}^2+E_{S1}E_{S0}\sin\phi. \quad (4)$$

These equations show that the maximum intensity of the two output signals have a phase difference of 180 degrees or π radians. Moreover, there is a phase delay (lag) of 90 degrees of $\pi/2$ radians with respect to the **S0** optical signal component that is part of the output signal propagating from the output waveguide Out1 relative to the **S0** optical signal component that is part of the output signal propagating from the output waveguide Out0.

As shown in FIG. **3**A, the three 180-degree optical hybrid couplers (**300**A, **300**B, **300**C) provide mixing of the received phase-shifted optical carrier signal and the optical LO signal output from the OPPL **122**. Two waveguides **301**A, **301**B

supply the received phased-shifted optical carrier signal and the optical LO signal to the In0 and the In1 input waveguides, respectively, of the first 180-degree optical hybrid coupler **300**A. In this configuration, the first 180-degree optical hybrid coupler **300**A mixes the received phase-shifted optical carrier signal and the optical LO signal to produce two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **300**A. The intensity of the two input optical signals is split evenly (50:50 split) in each one of two output signals with the maximum intensity of the two output signals having a phase difference of 180 degrees (π radians).

A waveguide **303**A supplies the output signal from the Out0 output waveguide of the 180-degree optical hybrid coupler **300**A to the In0 input waveguide of the 180-degree optical hybrid coupler **300**B. In this configuration, the 180-degree optical hybrid coupler **300**B produces two output signals that propagate out from the Out0 and the Out1 output waveguides of the 180-degree optical hybrid coupler **300**B. The intensity of the input signal is split evenly (50:50 split) in each one of two output signals with the maximum intensity of the two output signals having a phase difference of 180 degrees (π radians).

A waveguide **303**B supplies the output signal output from the Out1 output waveguide of the 180-degree optical hybrid coupler **300**A to the In0 input waveguide of 180-degree optical hybrid coupler **300**C. In this configuration, the 180-degree optical hybrid coupler **300**C produces two output signals that propagate out from the Out0 and Out1 output waveguides of the 180-degree hybrid coupler **300**C. The intensity of the input signal is split evenly (50:50 split) in each one of two output signals with the maximum intensity of the two output signals having a phase difference of 180 degrees (π radians).

Waveguides **305**A, **305**B, **305**C, **305**D supply the optical signals output from the Out0 and Out1 output waveguides of the 180-degree hybrid coupler **300**B as well as the optical signals output from the Out0 and Out1 output waveguides of the 180-degree hybrid coupler **300**C to corresponding phototransistors Q**1**, Q**2**, Q**3**, Q**4** of the thyristor-based optical phase detector as described below.

The thyristor-based optical phase detector includes a four terminal vertical thyristor (N region-P region-N region-P region) **307** with a split load. A first load element **309**A is coupled between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **307**. A second load element **309**B is coupled between the cathode terminal of the thyristor **307** and the negative voltage supply (ground). The thyristor **307** also has a p-channel injector terminal and an n-channel injector terminal.

A p-channel HFET phototransistor Q**1** and an n-channel HFET phototransistor Q**2** are coupled in series between the positive voltage supply (V_{cc}) and the negative voltage supply (ground). The p-channel HFET phototransistor Q**1** has a source and gate terminal both connected to the positive voltage supply (V_{cc}). The n-channel HFET phototransistor Q**2** has a source and gate terminal both connected to the negative voltage supply (ground). The drain of the p-channel HFET phototransistor Q**1** and the drain of the n-channel HFET phototransistor Q**2** are coupled together and to the p-channel injector terminal of the thyristor **307**.

A p-channel HFET phototransistor Q**3** and an n-channel HFET phototransistor Q**4** are coupled in series between the positive voltage supply (V_{cc}) and the negative voltage supply (ground). The p-channel HFET phototransistor Q**3** has a source and gate terminal both connected to the positive voltage supply (V_{cc}). The n-channel HFET phototransistor Q**4** has a source and gate terminal both connected to the negative voltage supply (ground). The drain of the p-channel HFET phototransistor Q**3** and the drain of the n-channel HFET phototransistor Q**4** are coupled together and to the n-channel injector terminal of the thyristor **307**.

The optical signal output from the Out0 output waveguide of the 180-degree optical hybrid coupler **300**B is guided into the waveguide region of the p-channel HFET phototransistor Q**1** and the optical signal output from the Out1 output waveguide of the 180-degree optical hybrid coupler is guided into the waveguide region of the p-channel HFET phototransistor Q**3**. The optical signal output from the Out0 output waveguide of the 180-degree optical hybrid coupler **300**C is guided into the waveguide region of the re-channel HFET phototransistor Q**2** and the optical signal output from the Out1 output waveguide of the 180-degree optical hybrid coupler **300**C is guided into the waveguide region of the n-channel HFET phototransistor Q**4**.

In this configuration, the phase of the optical carrier signal component that is part of the output signal propagating from the Out0 output waveguide of the 180-degree optical hybrid coupler **300**B (and supplied to the waveguide region of the p-channel HFET phototransistor Q**1**) is aligned (lag near 0 degrees or radians) to the phase of the received phase-shifted optical carrier signal. The optical carrier signal component that is part of the output signal propagating from the Out1 output waveguide of the 180-degree optical hybrid coupler **300**B (and supplied to the waveguide region of the p-channel HFET phototransistor Q**3**) lags in phase by 90 degrees ($\pi/2$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the optical carrier signal component that is part of the output signal propagating from the Out0 output waveguide of the 180-degree optical hybrid coupler **300**C (and supplied to the waveguide region of the n-channel HFET phototransistor Q**2**) lags in phase by 90 degrees ($\pi/2$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the optical carrier signal component that is part of the output signal propagating from the Out1 output waveguide of the 180-degree optical hybrid coupler **300**C (and supplied to the waveguide region of the n-channel HFET phototransistor Q**4**) lags in phase by 180 degrees (π radians) the phase of the received phase-shifted optical carrier signal.

Furthermore, in this configuration, the p-channel HFET phototransistor Q**1** and the n-channel HFET phototransistor Q**4** are activated and operate as turn-n phototransistors for the thyristor **307** when the phase of the received phase-shifted optical carrier signal corresponds to a first predefined phase offset (such as 0 degrees or radians). When activated, the p-channel HFET phototransistor Q**1** supplies hole current to the p-channel injector and the n-channel HFET phototransistor supplies electron current to the n-channel injector such that the thyristor **307** operates in its ON state where it conducts current vertically between the anode and the cathode terminal of the thyristor **307**. The p-channel HFET phototransistor Q**3** and the n-channel HFET phototransistor Q**2** are activated and operate as turn-off F phototransistors when the phase of the received phase-shifted optical carrier signal corresponds to a second predefined phase offset (such as 180 degrees or π radians). When activated, the p-channel HFET phototransistor Q**3** draws electron current from the n-channel injector and the n-channel HFET phototransistor Q**2** draws hole current from the p-channel injector such that the thyristor **307** operates in its OFF state where there is minimal conduction vertically between the anode and the cathode terminal of the thyristor **307**.

The ON and OFF states of the thyristor **307** generates digital (binary) electrical signals A, $\overline{A}$ at the cathode terminal and the anode terminal, respectively. Note that the digital

electrical signal A generated at the cathode terminal is complementary to the digital electrical signal $\overline{A}$ generated at the anode terminal. The ON state of the thyristor **307** can also be configured above the lasing threshold such that the thyristor **307** emits a digital (ON/OFF) optical signal corresponding to the digital electrical signal A generated at the cathode terminal of the thyristor **307**. In this configuration, the binary levels of the digital electrical signals A, $\overline{A}$ (and possibly the ON/OFF state of the digital optical signal emitted from the thyristor) for the ON and OFF states of the thyristor **307** correspond to the two possible phase offsets of the received phase-shifted optical carrier signal. An example of correspondence between the binary levels of the digital electrical signals A, $\overline{A}$ (and possibly the digital optical signal emitted by the thyristor) and two phase offsets of the received phase-shifted optical carrier signal is shown in the chart of FIG. **3**B and the phase constellation diagram of FIG. **3**C. Note that these two possible phase offsets are 180 degrees (or π radians) apart from one another.

QPSK and Higher Communication Systems

FIG. **4** shows an optical communication system **100'** employing optical QPSK (or higher order) phase shift keying signals. The transmitter **112'** is similar to the transmitter **112** for the BPSK system with the addition of a symbol encoder **117** that maps two sequential bits of the signal stream into a corresponding symbol phase. The optical PSK phase modulator **116'** modulates the phase of the optical carrier signal generated by the laser local oscillator **116** according to the symbol phase generated by the symbol encoder **117**. The optical PSK modulator **116'** can function to incorporate time delay into the optical signal path corresponding to the required phase change (as $\Delta\phi=\omega\Delta t$). This can be realized by a ring resonator where the effective optical velocity through the ring resonator is controlled in some manner (such as in response to one or more electrical signals supplied to the ring resonator). The phase-shifted optical carrier signal produced by the optical PSK modulator **116'** is carried by the communication medium (such as an optical fiber) to the receiver **120'**.

The receiver **120'** of the optical communication system **100'** is similar to the receiver **120** of the BPSK system including an OPPL **122** that functions to estimate and compensate for differences in oscillation frequency between the receiver's laser local oscillator and the optical carrier signal of the transmitter **112'**. It also aligns the phase of the receiver's laser local oscillator to the phase of the optical carrier signal of the transmitter **112'**. The optical local oscillating signal generated by the OPPL **122** along with the received optical phase-shifted carrier signal are processed by the optical PSK coherent demodulator **124'** to identify the phase offset of the received optical phased-shifted carrier signal relative to the optical local oscillating signal. This is a form of coherent homodyne detection of the phase information carried in the received phased-shifted optical carrier signal. The optical PSK coherent demodulator **124'** generates an electrical signal that encodes the symbol phase data corresponding to the phase offset information of the received phased-shifted optical carrier signal. The correspondence between the phase offset information and the symbol data values is dictated by the PSK modulation scheme employed by the optical PSK modulator **116'** of the transmitter **112'**. The optical PSK coherent demodulator **124'** also operates to generate an electrical clock signal (timing information) corresponding to the symbol clock of the transmitter **112'**. In this manner, the optical PSK coherent demodulator **124'** recovers the symbol phase data carried by the received phase-shifted optical carrier signal. The recovered phase data and the clock signal are supplied to a phase symbol decoder **128** that decodes the recovered phase symbol data to generate the binary signal stream represented by the symbol data. The binary signal stream is output by the symbol decoder **128** to circuitry **126'** that decodes the signal stream (if necessary) and performs serial-to-parallel data conversion. The parallel data (typically, byte-sizes chunks) can be output to a data processing circuit as needed.

FIG. **5** is a block diagram illustrating an embodiment of the receiver **120'** of FIG. **4**, which includes an OPPL **122**, an optical mixer and thyristor-based optical PSK detector **124**A', an optical clock recover block **124**B', a symbol decoder **128** and signal decode circuitry **126**. The OPPL **122** includes a laser local oscillator **201** and a loop filter **203**. The loop filter **203** functions to estimate and compensate for differences in oscillation frequency between the optical local oscillating signal generated by the laser local oscillator **201** and the optical carrier signal of the transmitter **112'**. The loop filter **203** also functions to align the phase of the optical local oscillating signal to the phase of the optical carrier signal of the transmitter **10**. The output of the laser local oscillator is supplied to a polarization control module **205** that is supplied to a polarization control module **205** that fixes the polarization state of the optical local oscillating signal to match the polarization of the received optical signal. This may be necessary as the laser local oscillator **201** may produce an optical polarization state that differs from the received optical signal.

The optical mixer and thyristor-based optical PSK detector **124**A' is configured to identify the phase offset of the received optical phased-shifted carrier signal relative to the optical local oscillating signal. This is form of coherent homodyne detection of the phase information carried in the received phased-shifted optical carrier signal. The optical mixer and thyristor-based optical PSK detector **124**A' generates an electrical signal that encodes the symbol data corresponding to the phase offset information of the received phased-shifted optical carrier signal. The correspondence between the phase offset information and the symbol data is dictated by the QPSK (or higher order) modulation scheme employed by the optical PSK modulator **116'** of the transmitter **112'**. In this manner, the optical mixer and thyristor-based optical PSK detector **124**A' recovers the signal stream of symbols carried by the received phase-shifted optical carrier signal.

The optical clock recovery block **124**B' operates to generate an electrical clock signal whose ON/OFF transitions are synchronized to the symbol clock of the transmitter **112'**. This symbol clock is embedded in the optical signal generated by the optical mixer and thyristor-based optical PSK detector **124**A', which represents the recovered signal stream of symbols carried by the received phase-shifted optical carrier signal and detected by the optical mixer and thyristor-based optical PSK detector **124**A'.

The signal decode circuitry **126** utilizes the electrical clock signal (recovered symbol clock) generated by the clock recovery block **124**B' to sample the symbol data generated by the optical mixer and thyristor-based optical PSK detector **124**A'. This symbol data represents the recovered signal stream of symbols carried by the received phase-shifted optical carrier signal and detected by the optical mixer and thyristor-based optical PSK detector **124**A'. This sampling is performed at the timing that corresponds recovered symbol clock and thus is aligned to the binary bit values carried by the received phase-shifted optical carrier signal. The signal decode circuitry **126** also performs signal decoding operations that map each recovered phase sample back to the binary symbol it represents and thus recovers the original data.

Optical QPSK Detector

An embodiment of the optical mixer and optical PSK detector **124**A' for detecting and demodulating optical QPSK signals is shown in FIG. **6**A. It employs a network of two 180-degree optical hybrid couplers **600**A and **600**B and two optical BPSK detectors **124**A-**1** and **124**A-**2** as described above with respect to FIG. **3**A for optical mixing and demodulation of the received phase-shifted carrier signal and the optical local oscillating signal output by the OPPL **122**. As shown in FIG. **6**A, one 180-degree optical hybrid coupler **600**A is used to split the received phase-shifted carrier signal for supply to the two optical BPSK detectors **124**A-**1** and **124**A-**2**. The other 180-degree optical hybrid coupler **600**B is used to split the optical local oscillating signal output by the OPPL **122** for supply to the two optical BPSK detectors **124**A-**1** and **124**A-**2**.

Waveguide **601**A supplies the received phased-shifted optical carrier signal to the In0 input waveguide of the 180-degree optical hybrid coupler **600**A. In this configuration, the 180-degree optical hybrid coupler **600**A produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **600**A. The intensity of the received phased-shifted optical carrier signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide.

Waveguide **601**B supplies the optical LO signal to the In0 input waveguide of the 180-degree optical hybrid coupler **600**B. In this configuration, the 180-degree optical hybrid coupler **600**B produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **600**B. The intensity of the optical LO signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide.

Waveguides **603**A and **603**C supply the optical signals output from the Out0 output waveguides of the 180-degree hybrid couplers **600**A and **600**B to the input waveguides **301**A and **301**B of the optical BPSK detector **124**A-**1** as shown. Waveguides **603**B and **603**D supply the optical signals output from the Out1 output waveguides of the 180-degree hybrid couplers **600**A and **600**B to the input waveguides **301**A and **301**B of optical BPSK detector **124**A-**2** as shown. In this configuration, the phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **603**A to the input waveguide **301**A of the optical BPSK detector **124**A-**1** is aligned in phase (lag near 0 degrees or radians) with the phase of the received phase-shifted optical carrier signal. The phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **603**B to the input waveguide **301**A of the optical BPSK detector **124**A-**2** lags by 90 degrees ($\pi/2$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the optical LO signal that is supplied via the waveguide **603**C to the input waveguide **301**B of the optical BPSK detector **124**A-**1** is aligned in phase (lag near zero degrees or radians) the phase of the optical LO signal produced by the OPPL **122**. The phase of the optical LO signal that is supplied via the waveguide **603**D to the input waveguide **301**B of the optical BPSK detector **124**A-**2** lags by 90 degrees ($\pi/2$ radians) the phase of the optical LO signal produced by the OPPL **122**.

The ON and OFF states of the thyristor **307** of the optical BPSK detector **124-1** generates digital electrical signals A, $\overline{A}$ at the cathode terminal and the anode terminal, respectively. Note that the digital electrical signal A generated at the cathode terminal is complementary to the digital electrical signal $\overline{A}$ generated at the anode terminal. The ON state of such thyristor **307** can also be configured above the lasing threshold such that the thyristor **307** emits a digital (ON/OFF) optical signal corresponding to the binary levels of the digital electrical signal A generated at the cathode terminal of the thyristor **307** of the optical BPSK detector **124-1**. The ON and OFF states of the thyristor **307** of the thyristor-based optical BPSK detector **124-2** generates digital electrical signals B, $\overline{B}$ at the cathode terminal and the anode terminal, respectively. Note that the digital electrical signal B generated at the cathode terminal is complementary to the digital electrical signal $\overline{B}$ generated at the anode terminal. The ON state of such thyristor **307** can also be configured above the lasing threshold such that the thyristor **307** emits a digital (ON/OFF) optical signal corresponding to the digital electrical signal B generated at the cathode terminal of the thyristor **307** of the optical BPSK detector **124-2**.

In this configuration, the binary levels of the digital electrical signals A, $\overline{A}$, B, $\overline{B}$ (and possibly the ON/OFF state of the digital optical signals emitted from the thyristors) for the ON and OFF states of the thyristors within the optical BPSK detectors **124-1** and **124-2** correspond to the four possible phase offsets of the received phase-shifted optical carrier signal. An example of correspondence between the binary levels of the digital electrical signals A, B (and possibly the ON/OFF state of the corresponding digital optical signals emitted from the thyristors) and four phase offsets of the received phase-shifted optical carrier signal is shown in the chart of FIG. **6**B and the phase constellation diagram of **7**C. Note that these two possible phase offsets are 90 degrees (or $\pi/2$ radians) apart from one another.

Optical 8-PSK Detector

An embodiment of the optical mixer and optical PSK detector **124**A" for detecting and demodulating optical 8-PSK signals is shown in FIG. **7**A. It employs a network of two 180-degree optical hybrid couplers **700**A and **700**B and two optical QPSK detectors **124**A'-**1** and **124**A'-**2** as described above with respect to FIG. **6**A for optical mixing of the received phase-shifted carrier signal and the optical local oscillating signal output by the OPPL **122** and demodulation. As shown in FIG. **7**A, the 180-degree optical hybrid coupler **700**A functions to split the received phase-shifted carrier signal for supply to the two optical QPSK detectors **124**A'-**1** and **124**A'-**2**. The 180-degree optical hybrid coupler **700**B functions to split the optical local oscillating signal output by the OPPL **122** for supply to the two optical QPSK detectors **124**A'-**1** and **124**A'-**2**.

Waveguide **701**A supplies the received phased-shifted optical carrier signal to the In0 input waveguide of the 180-degree optical hybrid coupler **700**A. In this configuration, the 180-degree optical hybrid coupler **700**A produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **700**A. The intensity of the received phased-shifted optical carrier signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide.

Waveguide **701**B supplies the optical LO signal to the In0 input waveguide of the 180-degree optical hybrid coupler **700**B. In this configuration, the 180-degree optical hybrid

coupler **700**B produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **700**B. The intensity of the optical LO signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide.

Waveguide **703**A supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **700**A to an optical phase modulator **705**, which functions to delay the phase of the supplied received phased-shifted optical carrier signal by 45 degrees (or $\pi/4$ radians). The resultant optical signal is supplied to the input waveguide **601**A of the optical QPSK detector **124**A'-**1** as shown. Waveguide **703**B supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **700**A to the input waveguide **601**A of the optical QPSK detector **124**A'-**2** as shown. Waveguide **703**C supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **700**B to the input waveguide **601**B of the optical QPSK detector **124**A'-**1** as shown. Waveguide **703**D supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **700**B to the input waveguide **601**B of the optical QPSK detectors **124**A'-**2** as shown.

In this configuration, the phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **703**A to the input waveguide **601**A of the optical QPSK detector **124**A'-**1** lags by 45 degrees ($\pi/4$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **703**B to the input waveguide **601**A of the optical QPSK detector **124**A'-**2** lags by 90 degrees ($\pi/2$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the optical LO signal that is supplied via the waveguide **703**C to the input waveguide **601**B of the optical QPSK detector **124**A'-**1** is aligned (lag near zero degrees or radians) to the phase of the optical LO signal supplied by the OPLL **122**. The phase of the optical LO signal that is supplied via the waveguide **703**D to the input waveguide **601**B of optical QPSK detector **124**A'-**2** lags by 90 degrees ($\pi/2$ radians) the phase of the optical LO signal that is supplied by the OPLL **122**.

Furthermore, in this configuration, the ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**1** generates digital electrical signals A, $\overline{A}$, B, $\overline{B}$ (and possibly corresponding digital optical signals A, B), and the ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**2** generates digital electrical signals A', $\overline{A}$', B', $\overline{B}$' (and possibly corresponding digital optical signals A', B'). The digital optical signals A', B' are supplied to a thyristor-based optical XOR block **707** that generates a digital electrical signal C that is the Boolean XOR function of the ON/OFF states of the digital optical signals A', B'. The binary levels of the digital electrical signals A, B, C correspond to the eight possible phase offsets of the received phase-shifted optical carrier signal. An example of correspondence between the binary levels of the electrical signals A, B, C and eight phase offsets of the received phase-shifted optical carrier signal is shown in the chart of FIG. **7**B and the phase constellation diagram of FIG. **7**C. Note that these eight possible phase offsets are 45 degrees (or $\pi/4$ radians) apart from one another.

Thyristor-Based Optical XOR Block

An embodiment of the thyristor-based optical XOR block **707** is shown in FIG. **8**A. It employs a network of two 180-degree optical hybrid couplers **800**A, **800**B for splitting the input digital optical signals A', B'. A waveguide **801**A supplies the input digital optical signal A' to the In0 input waveguide of 180-degree optical hybrid coupler **800**A. In this configuration, the 180-degree optical hybrid coupler **800**A produces two output signals that propagate out from the Out0 and the Out1 output waveguides of the 180-degree optical hybrid coupler **800**A. The intensity of the digital optical signal A' is split evenly (50:50 split) in each one of two output signals. A waveguide **801**B supplies the input digital optical signal B' to the In0 input waveguide of 180-degree optical hybrid coupler **800**B. In this configuration, the 180-degree optical hybrid coupler **800**B produces two output signals that propagate out from the Out0 and the Out1 output waveguides of the 180-degree optical hybrid coupler **800**B. The intensity of the digital optical signal B' is split evenly (50:50 split) in each one of two output signals.

Waveguides **803**A, **803**B, **803**C, **803**D supply the optical signals output from the Out0 and Out1 output waveguides of the 180-degree hybrid couplers **800**A and **800**B to corresponding phototransistors Q**1**, Q**2**, Q**3**, Q**4** of a thyristor-based circuit as described below.

The thyristor-based circuit includes a four terminal vertical thyristor (N region-P region-N region-P region) **807** with a split load. A first load element **809**A is coupled between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **807**. A second load element **809**B is coupled between the cathode terminal of the thyristor **807** and the negative voltage supply (ground). The thyristor **807** also has a p-channel injector terminal and an n-channel injector terminal.

A p-channel HFET phototransistor Q**1** and an n-channel HFET phototransistor Q**2** are coupled in series between the positive voltage supply (V_{cc}) and the negative voltage supply (ground). The p-channel HFET phototransistor Q**1** has a source and gate terminal both connected to the positive voltage supply (V_{cc}). The n-channel HFET phototransistor Q**2** has a source and gate terminal both connected to the negative voltage supply (ground). The drain of the p-channel HFET phototransistor Q**1** and the drain of the n-channel HFET phototransistor Q**2** are coupled together and to the p-channel injector terminal of the thyristor **807**.

A p-channel HFET phototransistor Q**3** and an n-channel HFET phototransistor Q**4** are coupled in series between the positive voltage supply (V_{cc}) and the negative voltage supply (ground). The p-channel HFET phototransistor Q**3** has a source and gate terminal both connected to the positive voltage supply (V_{cc}). The n-channel HFET phototransistor Q**4** has a source and gate terminal both connected to the negative voltage supply (ground). The drain of the p-channel HFET phototransistor Q**3** and the drain of the n-channel HFET phototransistor Q**4** are coupled together and to the re-channel injector terminal of the thyristor **807**.

The digital optical signal A' output from the Out0 output waveguide of the 180-degree optical hybrid coupler **800**A is guided into the waveguide region of the p-channel HFET phototransistor Q**1** and the digital optical signal A' output from the Out1 output waveguide of the 180-degree optical hybrid coupler **800**A is guided into the waveguide region of the p-channel HFET phototransistor Q**3**. The digital optical signal B' output from the Out0 output waveguide of the 180-degree optical hybrid coupler **800**B is guided into the waveguide region of the n-channel HFET phototransistor Q**2** and the digital optical signal B' output from the Out1 output waveguide of the 180-degree optical hybrid coupler **800**B is guided into the waveguide region of the n-channel HFET phototransistor Q**4**.

In this configuration, the p-channel HFET phototransistors Q**1** and Q**3** are activated when the state of the digital optical

signal A' is ON, and the n-channel HFET phototransistors Q2 and Q4 are activated when the state of the digital optical signal B' is ON. The p-channel HFET phototransistors Q1 is configured to operate as a turn-on phototransistor for the thyristor **807** when the state of the digital optical signal A' is ON and the state of the digital optical signal B' is OFF. The n-channel HFET phototransistor Q4 is configured to operate as a turn-on phototransistor for the thyristor **807** when the state of the digital optical signal B' is ON and the state of the digital optical signal A' is OFF. The p-channel HFET phototransistor Q3 and the n-channel HFET phototransistor Q2 are configured to operate as turn-off phototransistors for the thyristor **807** when the states of both the digital optical signal A' and the digital optical signal B' are ON.

Specifically, the phototransistors Q1, Q2, Q3 and Q4 can be sized so that the turn-off phototransistors Q2 and Q3 are larger (for example, by a factor of two) than the turn-on phototransistors Q1 and Q4. When the state of the digital optical signal A' is ON and the state of the digital optical signal B' is OFF, the p-channel HFET phototransistors Q1 and Q3 are activated and the n-channel HFET phototransistors Q2 and Q4 are not activated. In this case, the turn-on p-channel HFET phototransistor Q1 supplies hole current to the p-channel injector and the turn-off transistor Q3 draws electron current from the n-channel injector; however, due to the internal gain of the thyristor, the internal current flow of electrons is dominant which operates the thyristor **807** in its ON state where it conducts current vertically between the anode and the cathode terminal of the thyristor **807**. When the state of the digital optical signal A' is OFF and the state of the digital optical signal B' is ON, the p-channel HFET phototransistors Q1 and Q3 are not activated and the n-channel HFET phototransistors Q2 and Q4 are activated. In this case, the turn-on n-channel HFET phototransistor Q4 supplies electron current to the n-channel injector and the turn-off transistor Q2 draws hole current from the p-channel injector; however, due to the internal gain of the thyristor, the internal current flow of holes is dominant which operates the thyristor **807** in its ON state where it conducts current vertically between the anode and the cathode terminal of the thyristor **807**. When the states of both the digital optical signal A' and the digital optical signal B' are ON, the turn-on phototransistors Q1, Q2, Q3 and Q4 are all activated. However, in this case, the hole current drain operation of the larger turn-off transistor Q2 dominates the hole injection operation of the smaller turn-on transistor Q1, which effectively operates to drain hole current from the p-channel injector of the thyristor **807**. Similarly, the electron current drain operation of the larger turn-off transistor Q3 dominates the electron injection operation of the smaller turn-on transistor Q4, which effectively operates to drain electron current from the n-channel injector of the thyristor **807**. The drain of the hole current from the p-channel injector in conjunction with the drain of electron current from the n-channel injector operates the thyristor **807** in its OFF state where there is minimal current conduction vertically between the anode and the cathode terminal of the thyristor **807**. When the states of both the digital optical signals A' and B' are OFF, none of the phototransistors Q1, Q2, Q3, Q4 are activated and thyristor **807** operates in its OFF state.

The ON and OFF states of the thyristor **807** generates the digital electrical signal C at the cathode terminal of the thyristor **808**. The ON state of the thyristor **807** can also be configured above the lasing threshold such that the thyristor **807** emits a digital (ON/OFF) optical signal corresponding to the digital electrical signal C generated at the cathode terminal of the thyristor **807**. In this configuration, the binary levels of the digital electrical signal C (and possibly the ON/OFF state of the corresponding digital optical signal emitted from the thyristor) for the ON and OFF states of the thyristor **807** corresponds to the Boolean XOR function of the ON/OFF states of the digital optical signals A' and B' as shown in the table of FIG. **8**B.

Optical 16-PSK Detector

An embodiment of the optical mixer and optical PSK detector **124**A'" for detecting and demodulating optical 16-PSK signals is shown in FIGS. **9**A and **9**B. It employs a network of six 180-degree optical hybrid couplers **900**A, **900**B, **900**C, **900**D, **900**E and **900**F and four optical QPSK detectors **124**A'-**1**, **124**A'-**2**, **124**A'-**3**, **124**A'-**4** as described above with respect to FIG. **6**A for optical mixing of the received phase-shifted carrier signal and the optical local oscillating signal output by the OPPL **122** and demodulation.

As shown in FIG. **9**A, waveguide **901**A supplies the received phased-shifted optical carrier signal to the In0 input waveguide of the 180-degree optical hybrid coupler **900**A. In this configuration, the 180-degree optical hybrid coupler **900**A produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **900**A. The intensity of the received phased-shifted optical carrier signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide.

Waveguide **901**B supplies the optical LO signal to the In0 input waveguide of the 180-degree optical hybrid coupler **900**D. In this configuration, the 180-degree optical hybrid coupler **900**D produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **900**D. The intensity of the optical LO signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide.

Waveguide **903**A supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **900**A to an optical phase modulator **905**A, which functions to delay the phase of the supplied received phased-shifted optical carrier signal by 67.5 degrees (or $3\pi/8$ radians). The resultant optical signal is supplied by waveguide **903**C to the In0 input waveguide of the 180-degree optical hybrid coupler **900**B. In this configuration, the 180-degree optical hybrid coupler **900**B produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **900**B. The intensity of the resultant optical signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide. Waveguide **903**D supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **900**B to an optical phase modulator **905**B, which functions to delay the phase of the supplied received phased-shifted optical carrier signal by 45 degrees (or $\pi/4$ radians). The resultant optical signal is supplied by waveguide **903**E to the input waveguide **601**A of the optical QPSK detector **124**A'-**1**. Waveguide **903**F supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **900**B to the input waveguide **601**A of the optical QPSK detector **124**A'-**2**.

Waveguide **903**B supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **900**A to the In0 input waveguide of the 180-degree optical

hybrid coupler **900**C. In this configuration, the 180-degree optical hybrid coupler **900**C produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **900**C. The intensity of the resultant optical signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide. Waveguide **903**G supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **900**C to an optical phase modulator **905**C, which functions to delay the phase of the supplied received phased-shifted optical carrier signal by 45 degrees (or $\pi/4$ radians). The resultant optical signal is supplied by waveguide **903**H to the input waveguide **601**A of the optical QPSK detector **124**A'-**3**. Waveguide **903**I supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **900**C to the input waveguide **601**A of the optical QPSK detector **124**A'-**4**.

Waveguide **903**J supplies the optical LO signal output from the Out0 output waveguide of the 180-degree hybrid coupler **900**D to the In0 input waveguide of the 180-degree optical hybrid coupler **900**E. In this configuration, the 180-degree optical hybrid coupler **900**E produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **900**E. The intensity of the resultant optical signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide. Waveguide **903**L supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **900**E to the input waveguide **601**B of the optical QPSK detector **124**A'-**1**. Waveguide **903**M supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **900**E to the input waveguide **601**B of the optical QPSK detector **124**A'-**2**.

Waveguide **903**K supplies the optical LO signal output from the Out1 output waveguide of the 180-degree hybrid coupler **900**D to the In0 input waveguide of the 180-degree optical hybrid coupler **900**F. In this configuration, the 180-degree optical hybrid coupler **900**F produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **900**F. The intensity of the resultant optical signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees ($\pi/2$ radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide. Waveguide **903**N supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **900**F to the input waveguide **601**B of the optical QPSK detector **124**A'-**3**. Waveguide **903**O supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **000**F to the input waveguide **601**B of the optical QPSK detector **124**A'-**4**.

In this configuration, the phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **903**E to the input waveguide **601**A of the optical QPSK detector **124**A'-**1** lags by 112.5 degrees ($5\pi/8$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **903**F to the input waveguide **601**A of the optical QPSK detector **124**A'-**2** lags by 157.5 degrees ($7\pi/8$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **903**H to the input waveguide **601**A of the optical QPSK detector **124**A'-**3** lags by 135 degrees ($3\pi/4$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **903**I to the input waveguide **601**A of the optical QPSK detector **124**A'-**4** lags by 180 degrees (π radians) the phase of the received phase-shifted optical carrier signal. The phase of the optical LO signal that is supplied via the waveguide **903**L to the input waveguide **601**B of optical QPSK detector **124**A'-**1** is aligned (lag near zero degrees or radians) to the phase of the optical LO signal supplied by the OPLL **122**. The phase of the optical LO signal that is supplied via the waveguide **903**M to the input waveguide **601**B of optical QPSK detector **124**A'-**2** lags by 90 degrees ($\pi/2$ radians) the phase of the optical LO signal that is supplied by the OPLL **122**. The phase of the optical LO signal that is supplied via the waveguide **903**N to the input waveguide **601**B of optical QPSK detector **124**A'-**3** lags by 90 degrees ($\pi/2$ radians) the phase of the optical LO signal that is supplied by the OPLL **122**. The phase of the optical LO signal that is supplied via the waveguide **903**O to the input waveguide **601**B of optical QPSK detector **124**A'-**4** lags by 180 degrees (π radians) the phase of the optical LO signal that is supplied by the OPLL **122**.

Furthermore, in this configuration, the ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**1** generates digital electrical signals A, $\overline{A}$, B, $\overline{B}$ (and possibly corresponding digital optical signals A, B). The ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**2** generates digital electrical signals A', $\overline{A}$', B', $\overline{B}$' (and possibly corresponding digital optical signals A', B'). The ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**3** generates digital electrical signals a, $\overline{a}$, b, $\overline{b}$ (and possibly corresponding digital optical signals a, b). The ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**4** generates digital electrical signals a', $\overline{a}$', b', $\overline{b}$' (and possibly corresponding digital optical signals a', b').

As shown in FIG. **9**B, the digital optical signals A', B' are supplied to a thyristor-based optical XOR block **907**A that generates a digital electrical signal C (and possibly a corresponding digital optical signal C) that is the Boolean XOR function of the ON/OFF states of the digital optical signals A', B'. The digital optical signals a, b are supplied to a thyristor-based optical XOR block **907**B that generates a digital optical signal c (and possibly a corresponding digital optical signal c) that is the Boolean XOR function of the ON/OFF states of the digital optical signals a, b. The digital optical signals a', b' are supplied to a thyristor-based optical XOR block **907**C that generates a digital optical signal c' (and possibly a corresponding digital optical signal c) that is the Boolean XOR function of the ON/OFF states of the digital optical signals a', b'. The digital optical signals c, c' are supplied to a thyristor-based optical XOR block **907**D that generates a digital electrical signal D (and possibly a corresponding digital optical signal D) that is the Boolean XOR function of the ON/OFF states of the digital optical signals c, c'. The optical XOR blocks **907**A, **907**B, **907**D and **907**D can be realized with the optical XOR block described above with respect to FIGS. **8**A and **8**B.

The binary levels of the digital electrical signals A, B, C, D correspond to the sixteen possible phase offsets of the received phase-shifted optical carrier signal. An example of correspondence between the binary levels of the digital electrical signals A, B, C, D and four phase offsets of the received phase-shifted optical carrier signal is shown in the chart of FIG. **9**C and the phase constellation diagram of FIG. **9**D. Note

that these sixteen possible phase offsets are 22.5 degrees (or π/8 radians) apart from one another.

Optical 16-QAM Detector

An embodiment of the optical mixer and optical PSK detector **124**A"" for detecting and demodulating optical 16-QAM signals is shown in FIGS. **10**A and **10**B. It employs a network of six 180-degree optical hybrid couplers **1000**A, **1000**B, **1000**C, **1000**D, **1000**E and **1000**F and four optical QPSK detectors **124**A'-**1**, **124**A'-**2**, **124**A'-**3**, **124**A'-**4** as described above with respect to FIG. **6**A for optical mixing of the received phase-shifted carrier signal and the optical local oscillating signal output by the OPPL **122** and demodulation. The optical 16-QAM signals employ a combination of amplitude modulation (with four possible levels of amplitude modulation increasing in magnitude and designated T**1**, T**2**, T**3** and T**4**) and PSK modulation (with four possible phase offsets per amplitude modulation level). The Q**1** and Q**4** phototransistors of the four optical QPSK detectors operate to inject hole/electron current into corresponding thyristor injector terminals. Similarly, the Q**2** and Q**3** phototransistors of the four optical QPSK detectors operate to drain hole/electron current from the corresponding thyristor injector terminals. Furthermore, the supply voltages supplied to the thyristors of the four optical QPSK detectors are adjusted such that threshold levels for activating such thyristors increases in magnitude over the four optical QPSK detectors to correspond to the four possible levels of amplitude modulation T**1**, T**2**, T**3** and T**4**. In this manner, the threshold level for activation of the thyristor for the optical QPSK detector **124**A'-**1** is less than the threshold level for activation of the thyristor for the optical QPSK detector **124**A'-**2**, which is less than the threshold level for activation of the thyristor for the optical QPSK detector **124**A'-**3**, which is less than the threshold level for activation of the thyristor for the optical QPSK detector **124**A'-**4**. This configuration provides for optical detection and demodulation of the optical 16-QAM signals.

As shown in FIG. **10**A, waveguide **1001**A supplies the received phased-shifted optical carrier signal to the In0 input waveguide of the 180-degree optical hybrid coupler **1000**A. In this configuration, the 180-degree optical hybrid coupler **1000**A produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **1000**A. The intensity of the received phased-shifted optical carrier signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees (π/2 radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide.

Waveguide **1001**B supplies the optical LO signal to the In0 input waveguide of the 180-degree optical hybrid coupler **1000**D. In this configuration, the 180-degree optical hybrid coupler **1000**D produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **1000**D. The intensity of the optical LO signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees (π/2 radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide.

Waveguide **1003**A supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **1000**A to the In0 input waveguide of the 180-degree optical hybrid coupler **1000**B. In this configuration, the 180-degree optical hybrid coupler **1000**B produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **1000**B. The intensity of the resultant optical signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees (π/2 radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide. Waveguide **1003**C supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **1000**B to the input waveguide **601**A of the optical QPSK detector **124**A'-**1**. Waveguide **1003**D supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **1000**B to the input waveguide **601**A of the optical QPSK detector **124**A'-**2**.

Waveguide **1003**B supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **1000**A to the In0 input waveguide of the 180-degree optical hybrid coupler **1000**C. In this configuration, the 180-degree optical hybrid coupler **1000**C produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **1000**C. The intensity of the resultant optical signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees (π/2 radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide. Waveguide **1003**E supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **1000**C to the input waveguide **601**A of the optical QPSK detector **124**A'-**3**. Waveguide **1003**F supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **1000**C to the input waveguide **601**A of the optical QPSK detector **124**A'-**4**.

Waveguide **1003**G supplies the optical LO signal output from the Out0 output waveguide of the 180-degree hybrid coupler **1000**D to the In0 input waveguide of the 180-degree optical hybrid coupler **1000**E. In this configuration, the 180-degree optical hybrid coupler **1000**E produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **1000**E. The intensity of the resultant optical signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees (π/2 radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide. Waveguide **1003**I supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **1000**E to the input waveguide **601**B of the optical QPSK detector **124**A'-**1**. Waveguide **1003**J supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **1000**E to the input waveguide **601**B of the optical QPSK detector **124**A'-**2**.

Waveguide **1003**H supplies the optical LO signal output from the Out1 output waveguide of the 180-degree hybrid coupler **1000**D to the In0 input waveguide of the 180-degree optical hybrid coupler **1000**F. In this configuration, the 180-degree optical hybrid coupler **1000**F produces two output signals that propagate out from the Out0 and Out1 waveguides of the 180-degree optical hybrid coupler **1000**F. The intensity of the resultant optical signal is split evenly (50:50 split) in each one of two output signals with a phase delay (lag) of 90 degrees (π/2 radians) for the output signal that propagates out from the Out1 waveguide relative the output signal that propagates out from the Out0 waveguide. Waveguide **1003**K supplies the optical signal output from the Out0 output waveguide of the 180-degree hybrid coupler **1000**F to the input waveguide **601**B of the optical QPSK detector **124**A'-**3**. Waveguide **1003**L supplies the optical signal output from the Out1 output waveguide of the 180-degree hybrid coupler **1000**F to the input waveguide **601**B of the optical QPSK detector **124**A'-**4**.

In this configuration, the phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **1003**C to the input waveguide **601**A of the optical QPSK detector **124**A'-**1** is aligned (lag near zero degrees or radians) to the phase of the received phase-shifted optical carrier signal. The phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **1003**D to the input waveguide **601**A of the optical QPSK detector **124**A'-**2** lags by 90 degrees ($\pi/2$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **1003**E to the input waveguide **601**A of the optical QPSK detector **124**A'-**3** lags by 90 degrees ($\pi/2$ radians) the phase of the received phase-shifted optical carrier signal. The phase of the received phase-shifted optical carrier signal that is supplied via the waveguide **1003**F to the input waveguide **601**A of the optical QPSK detector **124**A'-**4** lags by 180 degrees (π radians) the phase of the received phase-shifted optical carrier signal. The phase of the optical LO signal that is supplied via the waveguide **1003**I to the input waveguide **601**B of optical QPSK detector **124**A'-**1** is aligned (lag near zero degrees or radians) to the phase of the optical LO signal supplied by the OPLL **122**. The phase of the optical LO signal that is supplied via the waveguide **1003**J to the input waveguide **601**B of optical QPSK detector **124**A'-**2** lags by 90 degrees ($\pi/2$ radians) the phase of the optical LO signal that is supplied by the OPLL **122**. The phase of the optical LO signal that is supplied via the waveguide **1003**K to the input waveguide **601**B of optical QPSK detector **124**A'-**3** lags by 90 degrees ($\pi/2$ radians) the phase of the optical LO signal that is supplied by the OPLL **122**. The phase of the optical LO signal that is supplied via the waveguide **1003**L to the input waveguide **601**B of optical QPSK detector **124**A'-**4** lags by 180 degrees (π radians) the phase of the optical LO signal that is supplied by the OPLL **122**.

As described above, the Q**1** and Q**4** phototransistors of the four optical QPSK detectors operate to inject hole/electron current into corresponding thyristor injector terminals. Similarly, the Q**2** and Q**3** phototransistors of the four optical QPSK detectors operate to drain hole/electron current from the corresponding thyristor injector terminals. Furthermore, the supply voltages supplied to the thyristors of the four optical QPSK detectors are adjusted such that threshold levels for activating such thyristors increases in magnitude over the four optical QPSK detectors to correspond to the four possible levels of amplitude modulation T**1**, T**2**, T**3** and T**4**.

In this configuration, the ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**1** generates digital electrical signals A**1**, A**1**, B**1**, B**1** (and possibly corresponding digital optical signals A**1**, B**1**) corresponding to four possible phase offsets for the T**1** level of amplitude modulation. The ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**2** generates digital electrical signals A**2**, A**2**, B**2**, B**2** (and possibly corresponding digital optical signals A**2**, B**2**) corresponding to four possible phase offsets for the T**2** level of amplitude modulation. The ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**3** generates digital electrical signals A**3**, $\overline{\text{A3}}$, B**3**, $\overline{\text{B3}}$ (and possibly corresponding digital optical signals A**3**, B**3**) corresponding to four possible phase offsets for the T**3** level of amplitude modulation. The ON and OFF states of the thyristors of the optical QPSK detector **124**A'-**4** generates digital electrical signals A**4**, $\overline{\text{A4}}$, B**4**, $\overline{\text{B4}}$ (and possibly corresponding digital optical signals A**4**, B**4**) corresponding to four possible phase offsets for the T**4** level of amplitude modulation. In this manner, the binary levels of the electrical signals A**1**, B**1**, A**2**, B**2**, A**3**, B**3**, A**4**, B**4** correspond to the sixteen possible combinations of amplitude modulation levels (T**1**/T**2**/T**3**/T**4**) and phase offsets of the received optical carrier signal.

An example of correspondence between the binary levels of the digital electrical signals A**1**, B**1**, A**2**, B**2**, A**3**, B**3**, A**4**, B**4** and sixteen combinations of amplitude modulation levels (T**1**/T**2**/T**3**/T**4**) and phase offsets of the received optical carrier signal is shown in the charts of FIGS. **10**C and **10**E and the phase constellation diagrams of FIGS. **10**D and **10**F. The chart of FIG. **10**C and the constellation diagram of FIG. **10**D show an example of correspondence between the binary levels of the electrical signals A**1**, B**1**, A**2**, B**2** and eight combinations of amplitude modulation levels (T**1**/T**2**) and phase offsets of the received optical carrier signal.

FIG. **10**E shows an embodiment for one part (the BPSK detector for the A**2** signal) of the optical QPSK detector **124**A'-**2** for the T**2** level of amplitude modulation. In this embodiment, the voltage supply potential (V_{T2}) is configured to set the switching threshold of the thyristor **307** (the point where the thyristor **307** operates in its ON state where it conducts current vertically between the anode and the cathode terminal of the thyristor **307**) such that is larger than the switching threshold for the thyristor **307** of the optical QPSK detector **124**A'-**1** for the T**1** level of amplitude modulation. A similar configuration is used for the other part (the BPSK detector for the B**2** signal) of the optical QPSK detector **124**A'-**2** for the T**2** level of amplitude modulation.

The chart of FIG. **10**F and the constellation diagram of FIG. **10**G show an example of correspondence between the binary levels of the digital electrical signals A**3**, B**3**, A**4**, B**4** and eight combinations of amplitude modulation levels (T**3**/T**4**) and phase offsets of the received optical carrier signal.

FIG. **10**H shows an embodiment for one part (the BPSK detector for the A**3** signal) of the optical QPSK detector **124**A'-**3** for the T**3** level of amplitude modulation. In this embodiment, the voltage supply potential (V_{T3}) is configured to set the switching threshold of the thyristor **307** such that is larger than the switching threshold for the thyristor **307** of the optical QPSK detector **124**A'-**2** for the T**2** level of amplitude modulation. A similar configuration is used for the other part (the BPSK detector for the B**3** signal) of the optical QPSK detector **124**A'-**3** for the T**3** level of amplitude modulation.

FIG. **10**I shows an embodiment for one part (the BPSK detector for the A**4** signal) of the optical QPSK detector **124**A'-**4** for the T**4** level of amplitude modulation. In this embodiment, the voltage supply potential (V_{T4}) is configured to set the switching threshold of the thyristor **307** such that is larger than the switching threshold for the thyristor **307** of the optical QPSK detector **124**A'-**2** for the T**3** level of amplitude modulation. A similar configuration is used for the other part (the BPSK detector for the B**4** signal) of the optical QPSK detector **124**A'-**4** for the T**4** level of amplitude modulation.

FIG. **10**J shows the combination of the constellation diagrams of FIGS. **10**D and **10**G to show the sixteen possible combinations of amplitude modulation levels (T**1**/T**2**/T**3**/T**4**) and phase offsets of the received optical carrier signal that can be represented by the binary levels of the digital electrical signals A**1**, B**1**, A**2**, B**2**, A**3**, B**3**, A**4**, B**4**. Note that the four possible phase offsets for each amplitude modulation level are 90 degrees (or $\pi/2$ radians) apart from one another.

Optical Phase Lock Loop/Clock Recovery Block

FIG. **11** is a block diagram illustrating an embodiment of the clock recovery block **124** of FIG. **2**B (and FIG. **5**), which is realized by an optical phase lock loop that includes a phase-tunable optoelectronic oscillator **1101**, an optical phase detector **1103** and an optical charge pump and loop filter circuit **1105**. The clock recovery block (particularly the optical phase detector **1103**) is supplied with a reference

optical signal input (in this example, the digital optical signal input **1111** generated by the PSK detector, which represents a recovered signal stream of symbols carried by a received phase-shifted optical carrier signal). The symbol clock employed by a transmitter in modulating the phase of the optical carrier signal is embedded in this digital optical signal input **1111**. The phase-tunable optoelectronic oscillator **1101** of the clock recovery block is configured to produce an optical clock signal (and corresponding electrical clock signal) having ON/OFF transitions that are synchronized to the timing of the reference optical signal input (in this example, the timing of symbol clock of the transmitter embedded in the digital optical signal input **1111**).

The optoelectronic oscillator **1101** produces an optical clock signal **1109**A and corresponding electrical clock signal **1109**B upon activation by a start signal **1107**. The phase of both the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B is tuned according to one or more phase tuning signals **1115** that are supplied to the optoelectronic oscillator **1101**. The digital optical signal input **1111** generated by the PSK detector as well as the optical clock signal **1109**A produced by the optoelectronic oscillator **1101** are supplied by waveguides to the optical phase detector **1103**, which functions to determine the digital phase difference (or equivalently to determine the difference in digital phase) between the digital optical signal input **1111** and the optical clock signal **1109**A and outputs one or more optical phase difference signals **1113** representative of such phase difference to the optical charge pump and loop filter **1105**. The optical charge pump and loop filter circuit **1005** functions as a loop filter to integrate the optical phase difference signals **1113** over time and generate the phase tuning signal(s) **1115** for control of the phase of the optical clock signal **1109**A (as well as the phase of the corresponding electrical clock signal **1109**B) such that it matches the phase of the symbol clock signal embedded within the digital optical signal input **1111**. In the locked state where the phase of the optical clock signal **1109**A (and the phase of the corresponding electrical clock signal **1109**B) matches the phase of the symbol clock signal, the frequency of the optical clock signal **1109**A (and the frequency of the corresponding electrical clock signal **1109**B) matches the frequency of the symbol clock signal. In this manner, the clock recovery block **124** operates to automatically tune the frequency and phase of the optical clock signal **1109**A (and the frequency and phase of the corresponding electrical clock signal **1109**B) into this locked state in order to recover the symbol clock signal embedded in the digital optical signal input **1111**.

The optical phase lock loop of FIG. **11** can be adapted to perform a wide variety of other functions beyond clock recovery. Such applications can include clock generation (such as up-conversion of a low frequency clock to a higher frequency clock or down-conversion of a higher frequency clock to a lower frequency clock), generation of local oscillating signals for communication systems (such as generation of local oscillating signals for modulation and demodulation), and clock distribution and jitter compensation in integrated circuits, instrumentation systems and communication systems.

Optical Phase Detector

FIG. **12**A illustrates an embodiment of the optical phase detector **1103** of FIG. **11**, which includes an AND gate **1205** operably coupled between two optical flip-flops **1203**A and **1203**B. The optical flip-flop **1203**A receives the digital optical signal input (D_A) **1111** at its D_A input and functions to generate a digital optical signal output Q_A and corresponding digital electrical signal output Q_A based on the binary level of the complementary digital electrical Reset/$\overline{\text{Reset}}$ signals at its R/$\overline{\text{R}}$ inputs and the digital optical signal input (D_A) **1111** at its D_A input according to the table of FIG. **12**B. The optical flip-flop **1203**B receives the optical clock signal (D_B) **1109**A at its D_B input and functions to generate a digital optical signal output Q_B and corresponding digital electrical signal output Q_B based on the binary level of the complementary digital electrical Reset/$\overline{\text{Reset}}$ signals at its R/R inputs and the clock signal (D_B) **1109**A at its D_B input according to table of FIG. **12**C. The AND gate **1205** receives the digital electrical output signals Q_A and Q_B output by the optical flip-flops **1203**A and **1203**B and generates the complementary electrical Reset/$\overline{\text{Reset}}$ signals according to the table of FIG. **12**D. The complementary electrical Reset/$\overline{\text{Reset}}$ signals are supplied to the R and $\overline{\text{R}}$ inputs of both optical flip-flops **1203**A and **1203**B.

In this configuration, the ON level of the digital optical signal input Q_A (and the corresponding high level of the digital electrical signal output Q_A) represents the digital phase difference between the digital optical signal input **1111** and the optical clock signal **1109**A (where the digital optical signal input **1111** is ON and the optical clock signal **1109**A is OFF). Similarly, the ON level of the digital optical signal output Q_B (and the corresponding high level of the electrical signal Q_B) represented the digital phase difference between the optical clock signal **1109**A and the digital optical signal input **1111** (where the optical clock signal **1109**A is ON and the digital optical signal input **1111** is OFF). The digital electrical and optical signal Q_A as well as the digital electrical and optical signals Q_B are output to the optical charge pump and filter circuit **1105**.

The optical charge pump and filter circuit **1105** operates as a loop filter that converts the digital optical signal Q_A into a corresponding voltage signal that tracks whether the digital optical signal output Q_A (and the corresponding digital electrical signal Q_A) is greater than the digital optical signal output Q_B (and the corresponding digital electrical signal Q_B) over time. This output is used as a phase tuning signal **1115** supplied to the optoelectronic oscillator **1101** in order to increase the frequency of the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101**. The optical charge pump and loop filter circuit **1105** also operates as a loop filter that converts the digital optical signal Q_B into a corresponding voltage signal that tracks whether the digital optical signal output Q_B (and the corresponding digital electrical signal Q_B) is greater than the digital optical signal output Q_A (and the corresponding digital electrical signal Q_A) over time. This output is used as a phase tuning signal **1115** supplied to the optoelectronic oscillator **1101** in order to decrease the frequency of the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101**. In this configuration, the frequency and phase of the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101** will be adjusted such that it matches the frequency and phase of the symbol clock for the recovered digital optical signal input **1111**.

FIG. **13**A illustrates an embodiment of the optical flip-flop **1203**A of FIG. **12**A. The optical flip-flop is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs (where at least one control input is an optical signal) and will have one or more outputs (where one or more of such outputs can be an optical signal). It can be used as basic storage element in sequential logic. It also can be used as a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems. When used in a finite-state machine, the

output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

A waveguide (not shown), which is the D_A input of the optical flip-flop **1203**A, supplies an optical control input signal (in this example, the recovered digital optical signal input **1111**) to the waveguide region of a four terminal vertical thyristor (N region-P region-N region-P region) **1300** with a split load. A first load element **1301**A is coupled between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **1300**. A second load element **1301**B is coupled between the cathode terminal of the thyristor **1300** and the negative voltage supply (ground). The thyristor **1300** also has a p-channel injector terminal and an n-channel injector terminal. A p-channel HFET transistor Q**1** is coupled between the positive voltage supply (V_{cc}) and the n-channel injector terminal. An n-channel HFET transistor Q**2** is coupled between the negative voltage supply (ground) and the p-channel injector terminal. Two complementary electrical control inputs (Reset/$\overline{\text{Reset}}$ signals), which in this example are output by the AND gate **1205**, are supplied as inputs to the optical flip-flop **1203**A. The electrical $\overline{\text{Reset}}$ signal is supplied as an input to the gate terminal of the p-channel HFET transistor Q**1**. The electrical Reset signal is supplied as an input to the gate terminal of the re-channel HFET transistor Q**2**. The p-channel HFET transistor Q**1** is activated and operates as a turn-off transistor for the thyristor **1300** when the level of the electrical $\overline{\text{Reset}}$ signal is low. The n-channel HFET transistor Q**2** is activated and operates as a turn-off transistor for the thyristor **1300** when the level of the electrical Reset signal is high. The complementary nature of the electrical Reset and $\overline{\text{Reset}}$ signals dictates that the p-channel HFET transistor Q**1** and the n-channel HFET transistor Q**2** are activated at the same time when the level of the electrical $\overline{\text{Reset}}$ signal is low and the level of the complementary electrical Reset signal is high. When activated, the p-channel HFET transistor Q**1** drains electron current from (i.e., supplies hole current to) the n-channel injector and the n-channel HFET transistor Q**2** drains hole current from (i.e., supplies electron current to) the p-channel injector of the thyristor **1300** such that the thyristor **1300** switches OFF and there is minimal current conduction between the anode terminal and the cathode terminal of the thyristor **1300**. When the electrical $\overline{\text{Reset}}$ signal is high (and the complementary electrical Reset signal is low) and the optical control input signal (in this example, the recovered digital optical signal input **1111**) is ON, the optical control input signal is absorbed by the thyristor **1300** in order to introduce majority charge carriers into the thyristor **1300**. Such absorbed charge is sufficient to operate the thyristor **1300** in its ON state where it conducts current vertically between the anode terminal and the cathode terminal of the thyristor **1300**. In this ON state, the current that conducts vertically between the anode terminal and the cathode terminal is above the lasing threshold of the thyristor **1300** in order to produce a digital optical signal Q_A that is emitted from the thyristor **1300**. A corresponding digital electrical signal Q_A is produced at the cathode terminal of the thyristor **1300**. Note that the current draining operations of the HFET transistors Q**1** and Q**2** that operate the thyristor **1300** in its OFF state in response to the electrical $\overline{\text{Reset}}$ signal being low (and the complementary electrical Reset signal being high) overrides the ON state operation of the thyristor **1300** triggered by the ON state of the optical control input signal. This arises because the HFET transistors Q**1** and Q**2** force the OFF state of the thyristor **1300**. In this manner, the ON and OFF states of the thyristor **1300** emits a digital (ON/OFF) optical signal Q_A and generates a corresponding digital electrical signal Q_A at the cathode terminal of the thyristor **1300**. The ON/OFF states of the digital optical signal Q_A and corresponding binary levels of the digital electrical signal Q_A correspond to the binary levels of the recovered digital optical signal **1111** (D_A) and the complementary electrical Reset/$\overline{\text{Reset}}$ signals according to the table of FIG. **12**B.

FIG. **13**B illustrates an embodiment of the optical flip-flop **1203**B of FIG. **12**A similar to the optical flip-flip of FIG. **13**A. A waveguide (not shown), which is the D_B input of the optical flip-flop **1203**B, supplies an optical control input signal (in this example, the optical clock signal **1009**A) to the waveguide region of a four terminal vertical thyristor (N region-P region-N region-P region) **1302** with a split load. A first load element **1303**A is coupled between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **1302**. A second load element **1303**B is coupled between the cathode terminal of the thyristor **1303** and the negative voltage supply (ground). The thyristor **1302** also has a p-channel injector terminal and an n-channel injector terminal. A p-channel HFET transistor Q**1** is coupled between the positive voltage supply (V_{cc}) and the n-channel injector terminal. An n-channel HFET transistor Q**2** is coupled between the negative voltage supply (ground) and the p-channel injector terminal. Two complementary electrical control inputs (Reset/$\overline{\text{Reset}}$ signals), which in this example are output by the AND gate **1205**, are supplied as inputs to the optical flip-flop **1203**B. The electrical $\overline{\text{Reset}}$ signal is supplied as an input to the gate terminal of the p-channel HFET transistor Q**1**. The electrical Reset signal is supplied as an input to the gate terminal of the n-channel HFET transistor Q**2**. The p-channel HFET transistor Q**1** is activated and operates as a turn-off transistor for the thyristor **1302** when the level of the electrical $\overline{\text{Reset}}$ signal is low. The n-channel HFET transistor Q**2** is activated and operates as a turn-off transistor for the thyristor **1302** when the level of the electrical Reset signal is high. The complementary nature of the electrical Reset and $\overline{\text{Reset}}$ signals dictates that the p-channel HFET transistor Q**1** and the n-channel HFET transistor Q**2** are activated at the same time when the level of the electrical $\overline{\text{Reset}}$ signal is low and the level of the complementary electrical Reset signal is high. When activated, the p-channel HFET transistor Q**1** drains electron current from (i.e., supplies hole current to) the n-channel injector and the n-channel HFET transistor Q**2** drains hole current from (i.e., supplies electron current to) the p-channel injector of the thyristor **1302** such that the thyristor **1302** switches OFF and there is minimal current conduction between the anode terminal and the cathode terminal of the thyristor **1302**. When the electrical $\overline{\text{Reset}}$ signal is high (and the complementary electrical Reset signal is low) and the optical control input signal (in this example, optical clock signal **1009**A) is ON, the optical control input signal is absorbed by the thyristor **1302** in order to introduce majority charge carriers into the thyristor **1302**. Such absorbed charge is sufficient to operate the thyristor **1302** in its ON state where it conducts current vertically between the anode terminal and the cathode terminal of the thyristor **1302**. In this ON state, the current that conducts vertically between the anode terminal and the cathode terminal is above the lasing threshold of the thyristor **1302** in order to produce a digital optical signal Q_B that is emitted from the thyristor **1302**. A corresponding digital electrical signal Q_B is produced at the cathode terminal of the thyristor **1302**. Note that the current draining operations of the HFET transistors Q**1** and Q**2** that operate the thyristor **1302** in its OFF state in response to the electrical $\overline{\text{Reset}}$ signal being low (and the complementary electrical Reset signal being high) overrides the ON state operation of

the thyristor **1302** triggered by the ON state of the optical control input signal. This arises because the HFET transistors Q1 and Q2 force the OFF state of the thyristor **1302**. In this manner, the ON and OFF states of the thyristor **1302** emits a digital (ON/OFF) optical signal Q_B and generates a corresponding digital electrical signal Q_B at the cathode terminal of the thyristor **1302**. The ON/OFF states of the digital optical signal Q_B and corresponding binary levels of the digital electrical signal Q_B correspond to the ON/OFF states of the optical clock signal **1009**A (D_B) and the complementary electrical Reset/$\overline{\text{Reset}}$ signals according to the table of FIG. **12**C.

FIG. **14**A illustrates an embodiment of an AND gate **1205** of FIG. **12** with electrical inputs. The AND gate **1205** is basic digital logic gate produces a digital electrical output signal (in this example, the electrical Reset signal) that is the logical conjunction (the Boolean AND function) of two digital electrical inputs (in this example, the digital electrical signals Q_A and Q_B) according to the table of FIG. **12**D. The AND gate **1205** includes a four terminal vertical thyristor (N region-P region-N region-P region) **1400** with a split load. A first load element **1401**A is coupled between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **1400**. A second load element **1401**B is coupled between the cathode terminal of the thyristor **1400** and the negative voltage supply (ground). The thyristor **1400** also has a p-channel injector terminal and an n-channel injector terminal.

A p-channel HFET transistor Q1 and an n-channel HFET transistor Q2 are coupled in series between the positive voltage supply (V_{cc}) and the negative voltage supply (ground). The p-channel HFET transistor Q1 has a source terminal connected to the positive voltage supply (V_{cc}). The n-channel HFET transistor Q2 has a source terminal connected to the negative voltage supply (ground). The drain terminal of the p-channel HFET transistor Q1 and the drain terminal of the n-channel HFET transistor Q2 are coupled together and to the n-channel injector terminal of the thyristor **1400**. An re-channel HFET transistor Q3 and a p-channel HFET transistor Q4 are coupled in series between the positive voltage supply (V_{cc}) and the negative voltage supply (ground). The n-channel HFET transistor Q3 has a drain terminal connected to the positive voltage supply (V_{cc}). The p-channel HFET transistor Q4 has a drain terminal connected to the negative voltage supply (ground). The source terminal of the n-channel HFET transistor Q3 and the source terminal of the p-channel HFET transistor Q4 are coupled together and to the p-channel injector terminal of the thyristor **1400**.

The digital electrical input Q_A (which is supplied from the optical flip-flop **1203**A in this example) is supplied as an input to the gate terminals of both the p-channel HFET transistor Q1 and the n-channel HFET transistor Q2. The digital electrical input Q_B (which is supplied from the optical flip-flop **1203**B in this example) is supplied as an input to the gate terminals of both the n-channel HFET transistor Q3 and the p-channel HFET transistor Q4. In this configuration, the n-channel HFET transistor Q2 is activated and operates as a turn-on transistor for the thyristor **1400** when the binary level of the digital electrical input Q_A is high. When activated, the n-channel HFET transistor Q2 supplies electron current to the n-channel injector. Similarly, the n-channel HFET transistor Q3 is activated and operates as a turn-on transistor for the thyristor **1400** when the binary level of the digital electrical input Q_B is high. When activated, the n-channel HFET transistor Q3 supplies hole current to the p-channel injector. The currents injected by both the n-channel HFET transistors Q2 and Q3 are configured such that the thyristor **1400** operates in its ON state where it conducts current vertically between the anode terminal and the cathode terminal of the thyristor **1400**.

The p-channel HFET transistor Q1 is activated and operates as a turn-off transistor for the thyristor **1400** when the binary level of the digital electrical input Q_A is low. When activated, the p-channel HFET transistor Q1 draws electron current from (i.e., supplies hole current to) the n-channel injector such that the thyristor **1400** operates in its OFF state where there is minimal current conduction vertically between the anode and the cathode terminal of the thyristor **1400**. Similarly, the p-channel HFET transistor Q4 is activated and operates as a turn-off transistor for the thyristor **1400** when the binary level of the digital electrical input Q_B is low. When activated, the p-channel HFET transistor Q4 draws hole current from (i.e., supplies electron current to) the p-channel injector such that the thyristor **1400** operates in its OFF state. Thus, when both of the digital electrical signals Q_A and Q_B are high, the thyristor **1400** operates in its ON state. When either one (but not both) of the digital electrical signals Q_A and Q_B are high, the thyristor **1400** operates in its OFF state. When either one (and possibly both) of the digital electrical signals Q_A and Q_B are low, the thyristor **1400** operates in its OFF state.

The ON and OFF states of the thyristor **1400** generates the digital electrical $\overline{\text{Reset}}$ signal at the anode terminal of the thyristor **1400** and a complementary Reset signal (of opposite polarity) at the cathode terminal of the thyristor **1400**. In this configuration, the binary levels of the digital electrical Reset signal for the ON and OFF states of the thyristor **1400** corresponds to the logical conjunction (the Boolean AND function) of two digital electrical inputs Q_A and Q_B according to the table of FIG. **12**D.

FIG. **14**B illustrates an embodiment of an AND gate **1205'** with optical inputs suitable for use in the circuit of FIG. **12**. The AND gate **1205'** is basic digital logic gate produces a digital electrical output signal (in this example, the electrical Reset signal) that is the logical conjunction of two digital optical inputs (in this example, the digital optical signals Q_A and Q_B) according to the table of FIG. **12**D. The AND gate **1205'** includes a four terminal vertical thyristor (N region-P region-N region-P region) **1400'** with a split load. A first load element **1403**A is coupled between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **1400'**. A second load element **1403**B is coupled between the cathode terminal of the thyristor **1400'** and the negative voltage supply (ground). The thyristor **1400'** also has a p-channel injector terminal and an n-channel injector terminal.

A p-channel HFET transistor Q1 is coupled between the positive voltage supply (V_{cc}) and the n-channel injector terminal of the thyristor **1400'**. The source terminal and gate terminal of the p-channel HFET transistor Q1 are connected to the positive voltage supply (V_{cc}). The drain terminal of the p-channel HFET transistor Q1 is coupled to the n-channel injector terminal of the thyristor **1400'**. An n-channel HFET transistor Q2 is coupled between the negative voltage supply (ground) and the p-channel injector terminal of the thyristor **1400'**. The source terminal and gate terminal of the re-channel HFET transistor Q2 are connected to the negative voltage supply (ground). The drain terminal of the n-channel HFET transistor Q2 is coupled to the p-channel injector terminal of the thyristor **1400'**.

Waveguides (not shown) supply both the digital optical inputs Q_A and Q_B to the waveguide region of the thyristor **1400'**. In this configuration, the digital optical inputs Q_A and Q_B are absorbed by the thyristor **1400'** in order to introduce majority charge carriers into the thyristor **1400'**. When both the digital optical inputs Q_A and Q_B are in the ON state, such absorbed charge is sufficient to operate the thyristor **1400'** in its ON state where it conducts current vertically between

anode terminal and the cathode terminal of the thyristor **1400'**. The p-channel HFET transistor **Q1** and the n-channel HFET transistor **Q2** operate as a turn-off transistors for the thyristor **1400'** when either one (but not both) of the digital optical inputs Q_A and Q_B are in the ON state such that the thyristor **1400** operates in its OFF state where there is minimal current conduction vertically between the anode and the cathode terminal of the thyristor **1400'**. In the ON state of the thyristor **1400'**, the current that conducts vertically between anode terminal and the cathode terminal of the thyristor **1400'** generates the digital $\overline{\text{Reset}}$ output at the anode terminal of the thyristor **1400'** and the complementary Reset output (of opposite polarity) at the cathode terminal of the thyristor **1400'**. The bias configuration of the p-channel HFET transistor **Q1** and the n-channel HFET transistor **Q2** also operates the thyristor **1400'** in its OFF state when both the digital optical signals Q_A and Q_B are in the OFF state. The ON and OFF states of the thyristor **1400'** generates the digital $\overline{\text{Reset}}$ output at the anode terminal of the thyristor **1400'** and the complementary Reset output (of opposite polarity) at the cathode terminal of the thyristor **1400'**. In this configuration, the binary levels of the digital Reset output for the ON and OFF states of the thyristor **1400'** corresponds to the logical conjunction (the Boolean AND function) of two digital electrical inputs Q_A and Q_B according to the table of FIG. **12**D.

Optical Charge Pump

FIG. **15**A illustrates an embodiment of an optical charge pump and filter circuit **1105** for use in the circuit of FIG. **11**. The optical charge pump and filter circuit **1105** operates as a switched current source and loop filter where positive and negative current pulses are injected into two corresponding loop filter stages, where one loop filter stage outputs an electrical control output (control D signal) that is used to introduce a positive change in frequency to the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101**, and where the other loop filter stage outputs an electrical control output (control C signal) that is used to introduce a negative change in frequency to the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101**.

The optical charge pump and filter circuit **1105** includes two four terminal vertical thyristor (N region-P region-N region-P region) **1500** and **1504** each with a split load. For the thyristor **1500**, a first load element **1501**A is coupled between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **1500**. A second load element **1501**B and a capacitor **1503** are coupled in parallel between the cathode terminal of the thyristor **1500** and the negative voltage supply (ground). The parallel arrangement of the second load element **1501**B and the capacitor **1503** coupled between the cathode terminal of the thyristor **1500** and the negative voltage supply (ground) functions as a loop filter stage that outputs an electrical control output (control D signal) that is used to introduce a positive change in frequency to the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101**. The thyristor **1500** also has a p-channel injector terminal and an n-channel injector terminal. An n-channel HFET transistor **Q1** is coupled between the positive voltage supply (V_{cc}) and the n-channel injector terminal of the thyristor **1500**. The drain terminal of the n-channel HFET transistor **Q1** is connected to the positive voltage supply (V_{cc}). The source terminal of the n-channel HFET transistor **Q1** is coupled to the re-channel injector terminal of the thyristor **1500**. An n-channel HFET transistor **Q2** is coupled between the negative voltage supply (ground) and the p-channel injector terminal of the thyristor **1500**. The source terminal of the n-channel HFET transistor **Q2** is connected to the negative voltage supply (ground). The drain terminal of the n-channel HFET transistor **Q2** is coupled to the p-channel injector terminal of the thyristor **1500**. A waveguide (not shown) supplies the digital optical input Q_A as input to the waveguide region of the thyristor **1500**. The digital electrical input Q_B is supplied as input to the gate terminals of the n-channel HFET transistors **Q1** and **Q2**.

For the thyristor **1504**, a first load element **1505**A and a capacitor **1506** are coupled in parallel between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **1504**. The parallel arrangement of the first load element **1505**A and the capacitor **1506** coupled between the positive voltage supply and the anode terminal of the thyristor **1504** functions as a loop filter stage that outputs an electrical control output (control C signal) that is used to introduce a negative change in frequency to the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101**. A second load element **1505**B is coupled between the cathode terminal of the thyristor **1504** and the negative voltage supply (ground). The thyristor **1504** also has a p-channel injector terminal and an n-channel injector terminal. An n-channel HFET transistor **Q3** is coupled between the positive voltage supply (V_{cc}) and the n-channel injector terminal of the thyristor **1504**. The drain terminal of the re-channel HFET transistor **Q3** is connected to the positive voltage supply (V_{cc}). The source terminal of the n-channel HFET transistor **Q3** is coupled to the n-channel injector terminal of the thyristor **1504**. An n-channel HFET transistor **Q4** is coupled between the negative voltage supply (ground) and the p-channel injector terminal of the thyristor **1504**. The source terminal of the n-channel HFET transistor **Q4** is connected to the negative voltage supply (ground). The drain terminal of the n-channel HFET transistor **Q4** is coupled to the p-channel injector terminal of the thyristor **1504**. A waveguide (not shown) supplies the digital optical signal Q_B as input to the waveguide region of the thyristor **1504**. The digital electrical input Q_A is supplied as input to the gate terminals of the n-channel HFET transistors **Q3** and **Q4**.

In this configuration, the ON level of the digital optical signal Q_A input (and the corresponding high level of the digital electrical signal Q_A input) represents the phase difference between the recovered digital optical signal **1111** and the clock signal **1109**A (where the recovered digital optical signal **1111** is ON and the clock signal **1109**A is OFF). Similarly, the ON level of the digital optical signal Q_B input (and the corresponding high level of the digital electrical signal Q_B input) represents the phase difference between the clock signal **1109**A and the recovered digital optical signal **1111** (where the clock signal **1109**A is ON and the recovered digital optical signal **1111** is OFF).

The thyristor **1500** absorbs the digital optical signal Q_A to introduce majority charge carriers in the thyristor **1500**. The digital electrical signal Q_B supplied as input to the gate terminal of the n-channel HFET transistor **Q1** selectively activates (or deactivates) the drain-source current path of the n-channel HFET transistor **Q1**. When the digital electrical signal Q_B is high, the drain-source current path of the n-channel HFET transistor **Q1** is activated to drain electrons from the n-channel injector of the thyristor **1500**. When the digital electrical signal Q_B is low, the drain-source current path of the n-channel HFET transistor **Q1** is deactivated such that there is minimal conduction from the n-channel injector of the thyristor **1500**. Similarly, the digital electrical signal Q_B supplied as input to the gate terminal of the n-channel HFET transistor **Q2** selectively activates (or deactivates) the drain-source cur-

rent path of the n-channel HFET transistor Q2. When the digital electrical input Q_B is high, the drain-source current path of the re-channel HFET transistor Q2 is activated to drain holes from the p-channel injector of the thyristor **1500**. When the digital electrical signal Q_B is low, the drain-source current path of the n-channel HFET transistor Q2 is deactivated such that there is minimal conduction from the p-channel injector of the thyristor **1500**. Thus, with the digital electrical signal Q_B being high, the n-channel HFET transistors Q1 and Q2 are activated to drain majority carriers from the thyristor **1500** and counteract the introduction of majority carriers into the thyristor as a result of absorption of the digital optical signal Q_A. In this configuration, the thyristor **1500** switches ON to provide positive current that flows to the RC load provided by the parallel load **1501**B and capacitor **1503** only when the digital optical signal Q_A is ON and the digital electrical signal Q_B is low (i.e., the corresponding digital optical signal Q_B is OFF). With the thyristor **1500** in the ON state, the voltage potential of the cathode terminal of the thyristor **1500** increases and the RC load provided by the parallel load **1501**B and capacitor **1503** operates as a filter stage that integrates such increases in the voltage potential of the cathode terminal over time. The result of such integration is an increasing voltage signal at the cathode terminal whose change over time tracks the phase offset of the digital optical signal Q_A relative to the digital optical signal Q_B over time. An example of the increasing voltage signal generated at the cathode terminal of the thyristor **1500** is shown in FIG. **15**B. The cathode terminal voltage signal of the thyristor **1500** is used as a Control D signal that is output and supplied to the optoelectronic oscillator **1101** in order to introduce a positive change in frequency to the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101**.

The thyristor **1504** absorbs the digital optical signal Q_B to introduce majority charge carriers in the thyristor **1504**. The digital electrical signal Q_A supplied as input to the gate terminal of the n-channel HFET transistor Q3 selectively activates (or deactivates) the drain-source current path of the n-channel HFET transistor Q3. When the digital electrical signal Q_A is high, the drain-source current path of the n-channel HFET transistor Q3 is activated to drain electrons from the n-channel injector of the thyristor **1504**. When the digital electrical signal Q_A is low, the drain-source current path of the n-channel HFET transistor Q3 is deactivated such that there is minimal conduction from the n-channel injector of the thyristor **1504**. Similarly, the digital electrical signal Q_A supplied as input to the gate terminal of the n-channel HFET transistor Q4 selectively activates (or deactivates) the drain-source current path of the n-channel HFET transistor Q4. When the digital electrical signal Q_A is high, the drain-source current path of the n-channel HFET transistor Q4 is activated to drain holes from the p-channel injector of the thyristor **1504**. When the digital electrical signal Q_A is low, the drain-source current path of the n-channel HFET transistor Q4 is deactivated such that there is minimal conduction from the p-channel injector of the thyristor **1504**. Thus, with the digital electrical signal Q_A being high, the n-channel HFET transistors Q3 and Q4 are activated to drain majority carriers from the thyristor **1504** and counteract the introduction of majority carriers into the thyristor as a result of absorption of the digital optical signal Q_B. In this configuration, the thyristor **1504** switches ON to provide negative current that flows out of the RC load provided by the parallel load **1505**A and capacitor **1506** only when the digital optical signal Q_B is ON and the digital electrical signal Q_A is low (i.e., the corresponding digital optical signal Q_A is OFF). With the thyristor **1504** in the ON state, the voltage potential of the anode terminal of the thyristor **1504** decreases and the RC load provided by the parallel load **1505**A and capacitor **1506** operates as a filter stage that integrates such decreases in the voltage potential of the anode terminal over time. The result of such integration is a decreasing voltage signal at the anode terminal whose change over time tracks the phase offset of the digital optical signal Q_B relative to the digital optical signal Q_A over time. An example of the decreasing voltage signal generated at the anode terminal of the thyristor **1504** is shown in FIG. **15**C. The anode terminal voltage signal of the thyristor **1504** is used as a Control C signal that is output and supplied to the optoelectronic oscillator **1101** in order to introduce a negative change to the frequency of the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101**.

In this configuration, the control signals C and D dynamically adjust the frequency and phase of the optical clock signal **1109**A and the corresponding electrical clock signal **1109**B generated by the optoelectronic oscillator **1101** such that it matches the frequency and phase of the symbol clock embedded in the recovered optical signal when it achieved the phase/frequency locked condition. This phase/frequency locked condition is achieved when the C and D control signals become constant (independent of time). This locked condition is not shown in FIGS. **15**B and **15**C.

Optoelectronic Oscillator

FIG. **16** shows an embodiment of an optoelectronic oscillator **1101** suitable for use in the circuit of FIG. **11**. The optoelectronic oscillator **1101** produces an oscillating optical output signal and corresponding oscillating electrical output signal (i.e., an optical clock signal **1109**A and the corresponding electrical clock signal **1109**B in the example herein) whose oscillation frequency is controlled by two electrical input signals. One electrical input signal (i.e., the Control C signal in the example herein) introduces a negative change to the oscillation frequency of the oscillating optical output signal (and corresponding oscillating electrical output signal). The other electrical input signal (i.e., the Control D signal in the example herein) introduces a positive change to the oscillation frequency of the oscillating optical output signal (and corresponding oscillating electrical output signal).

The optoelectronic oscillator **1101** includes a four terminal vertical thyristor (N region-P region-N region-P region) **1600** with a p-channel injector terminal and an n-channel injector terminal. An n-channel HFET transistor Q1 is coupled between the positive voltage supply (V_{cc}) and the anode terminal of the thyristor **1600**. A p-channel HFET transistor Q2 is coupled between the positive voltage supply (V_{cc}) and the n-channel injector terminal of the thyristor **1500**. The source terminal of p-channel HFET transistor Q2 is connected to the positive voltage supply (V_{cc}). The drain terminal of the p-channel HFET transistor Q2 is coupled to the n-channel injector terminal. A p-channel HFET transistor Q3 is coupled between the negative voltage supply (ground) and the p-channel injector terminal of the thyristor **1600**. The drain terminal of the p-channel HFET transistor Q3 is connected to the negative voltage supply (ground). The source terminal of the p-channel HFET transistor Q3 is coupled to the p-channel injector terminal of the thyristor **1600**. An n-channel HFET transistor Q4 is coupled between the cathode terminal of the thyristor **1500** and the negative voltage supply (ground).

A feedback waveguide **1603** is coupled to the waveguide region of the thyristor **1600**. The waveguide region of the thyristor **1600** acts as an optical pulse regenerator that emits an output optical pulse in response to a detected input optical

pulse. An electrical output pulse corresponding the output optical pulse is generated at the cathode terminal of the thyristor **1600**. The feedback waveguide structure **1603** splits the output optical pulse into two parts. One part is output from the feedback waveguide structure **1603** to form a train of optical pulses that defines the output optical clock signal. The other part is guided by the feedback waveguide **1603** such that it returns back to the thyristor **1600** as an input optical pulse to produce another output optical pulse. Such optical pulse regeneration can be initiated by an electrical start-up pulse signal that is supplied to the n-channel injector of the thyristor as shown. The corresponding electrical pulse train generated at the cathode terminal of the thyristor **1600** is output as the electrical clock signal. A semiconductor optical amplifier **1605** can be integral to the feedback waveguide **1603** and configured to amplify the optical pulse signal guided by the feedback waveguide. Such amplification can compensate for losses in splitting off the optical clock signal from the circuit.

The pulse width of the output optical pulse (and corresponding output electrical pulse) is given by:

$$t_{pulse}=t_{intrinsic}+t_{trigger}. \quad (5)$$

The parameter $t_{intrinsic}$ is the intrinsic time delay of the device, which is based upon fabrication and growth parameters of the device (and is typically on the order of 1 to 4 picoseconds). The parameter $t_{trigger}$ is related to the effective area of the thyristor **1600**, threshold charge density, and the charging current as follows:

$$A*\sigma_{trigger}=Q_{trigger}=I_{trigger}*t_{trigger}. \quad (6)$$

The parameter A is the effective area of thyristor **1600**. The parameter $\sigma_{trigger}$ is the threshold charge density. The parameter $Q_{trigger}$ is the threshold charge. The parameter $I_{trigger}$ is the charging or trigger current.

The trigger current $I_{trigger}$ relates to the optically induced photocurrent and the bias current as follows:

$$I_{trigger}=I_{input}-I_{BiasN}-I_{BiasP} \quad (7)$$

The parameter I_{input} is the optically induced photocurrent produced by absorption of the input optical pulse. I_{BiasN} is the electron current drawn from the n-channel injector of the thyristor **1600**. I_{BiasP} is the hole current drawn from the p-channel injector of the thyristor **1600**.

The optically induced photocurrent I_{input} is given by:

$$I_{input}=\eta_i*P_{input} \quad (8)$$

The parameter represents the quantum efficiency of the thyristor **1600**. The parameter P_{input} is the power of input optical pulse.

Solving equation (6) for the parameter $t_{trigger}$ using equations (7) and (8) for the parameter $I_{trigger}$ yields:

$$t_{trigger} = Q_{trigger} / I_{trigger}, \text{ and} \quad (9)$$

$$t_{trigger} = \frac{A * \sigma_{trigger}}{(\eta_i * P_{input}) - I_{BiasN} - I_{BiasP}}. \quad (10)$$

From inspection of equations (10), (9) and (5), if the optical power of input optical pulse is held constant (P_{input} is constant), an increase in the bias current I_{BiasN} leads to a decrease in $I_{trigger}$, an increase in $t_{trigger}$, and an increase in t_{pulse}. The increase in t_{pulse} decreases the frequency of the output optical pulse train emitted from the thyristor **1600** that forms the optical clock signal and the matching frequency of the corresponding output electrical pulse train generated at the cathode terminal of the thyristor **1600** that forms the electrical clock signal. In contrast, a decrease in the bias current I_{BiasP} leads to an increase in $I_{trigger}$, a decrease in $t_{trigger}$, and a decrease in t_{pulse}. The decrease in t_{pulse} increases the frequency of the output optical pulse train emitted from the thyristor **1600** that forms the optical clock signal and the matching frequency of the corresponding output electrical pulse train generated at the cathode terminal of the thyristor **1600** that forms the electrical clock signal.

Moreover, from the inspection of equations (10), (9) and (5), if the bias currents I_{BiasN} and I_{BiasP} are held constant, a decrease in the optical power of the input optical pulse (decrease in P_{input}) leads to a decrease in $I_{trigger}$, an increase in trigger, and an increase in t_{pulse}. The increase in t_{pulse} decreases the frequency of the output optical pulse train emitted from the thyristor **1600** that forms the optical clock signal and the matching frequency of the corresponding output electrical pulse train generated at the cathode terminal of the thyristor **1600** that forms the electrical clock signal. In contrast, an increase in the optical power of the input optical pulse (increase in P_{input}) leads to an increase in $I_{trigger}$, a decrease in $t_{trigger}$, and a decrease in t_{pulse}. The decrease in t_{pulse} increases the frequency of the output optical pulse train emitted from the thyristor **1600** that forms the optical clock signal and the matching frequency of the corresponding output electrical pulse train generated at the cathode terminal of the thyristor **1600** that forms the electrical clock signal.

These relationships are exploited to control the frequency of the output optical pulse train emitted from the thyristor **1600** that forms the optical clock signal and the corresponding output electrical pulse train generated at the cathode terminal of the thyristor **1600** that forms the electrical clock signal.

Specifically, the C control signal (which can be generated by the optical charge pump **1105** as described in the example above) is supplied as input to the gate terminals of the HFET transistors Q**1** and Q**2**, and the D control signal (which can be generated by the optical charge pump **1105** as described in the example above) is supplied as input to the gate terminals of the HFET transistors Q**3** and Q**4**. The C control signal as supplied to the gate terminal of the n-channel HFET transistor Q**1** controls the variable source-drain resistance of the transistor Q**1**. A decrease in the C control signal increases the source-drain resistance of the transistor Q**1** and thus decreases the ON state voltage drop across the thyristor **1600**, thereby decreasing the power level of the output optical pulse. This decrease in power level results in a decrease in the optical power of the input optical pulse (decrease in P_{input}) that is returned to the thyristor **1600**. The C control signal as supplied to the gate terminal of the p-channel HFET transistor Q**2** controls the variable source-drain resistance of the transistor Q**2**. A decrease in the C control signal decreases the source-drain resistance of the transistor Q**2** and thus increases the bias current I_{BiasN}. Thus, a decrease in the C control signal results in a decrease in the optical power of the input optical pulse (decrease in P_{input}) as well as an increase in the bias current I_{BiasN}. Both of these conditions decrease the frequency of the output optical pulse train emitted from the thyristor **1600** that forms the optical clock signal and the matching frequency of the corresponding output electrical pulse train generated at the cathode terminal of the thyristor **1600** that forms the electrical clock signal.

The D control signal as supplied to the gate terminal of the n-channel HFET transistor Q**4** controls the variable source-drain resistance of the transistor Q**4**. An increase in the D control signal lowers the source-drain resistance of the transistor Q**4** and thus increases the ON state voltage drop across the thyristor **1600**, thereby increasing the power level of the

output optical pulse. This increase in power level results in an increase in the optical power of the input optical pulse (increase in P_{input}) that is returned to the thyristor **1600**. The D control signal as supplied to the gate terminal of the p-channel HFET transistor Q**3** controls the variable source-drain resistance of the transistor Q**3**. An increase in the D control signal increases the source-drain resistance of the transistor Q**3** and thus decreases the bias current I_{BiasP}. Thus, an increase in the D control signal results in an increase in the optical power of the input optical pulse (increase in P_{input}) as well as a decrease in the bias current I_{BiasP}. Both of these conditions increase the frequency of the output optical pulse train emitted from the thyristor **1600** that forms the optical clock signal and the matching frequency of the corresponding output electrical pulse train generated at the cathode terminal of the thyristor **1600** that forms the electrical clock signal.

In this configuration, the frequency and phase of the optical clock signal and the corresponding electrical clock signal are adjusted dynamically by decreases in the control signal C and increases in the control signal D.

POET Building Blocks

The electronic circuit components (such as the HFET transistors and electrical thyristors) as well as the optoelectronic circuit components (such as the optical hybrid couplers and optical thyristors) of the circuits as described herein can be implemented in one or more integrated circuits based on technology (referred to by the Applicant as "Planar Optoelectronic Technology" or "POET"). POET provides for the realization of a variety of devices (optoelectronic devices, logic circuits and/or signal processing circuits) utilizing inversion quantum-well channel device structures as described in detail in U.S. Pat. No. 6,031,243; U.S. patent application Ser. No. 09/556,285, filed on Apr. 24, 2000; U.S. patent application Ser. No. 09/798,316, filed on Mar. 2, 2001; International Application No. PCT/US02/06802 filed on Mar. 4, 2002; U.S. patent application Ser. No. 08/949,504, filed on Oct. 14, 1997, U.S. patent application Ser. No. 10/200,967, filed on Jul. 23, 2002; U.S. application Ser. No. 09/710,217, filed on Nov. 10, 2000; U.S. Patent Application No. 60/376,238, filed on Apr. 26, 2002; U.S. patent application Ser. No. 10/323,390, filed on Dec. 19, 2002; U.S. patent application Ser. No. 10/280,892, filed on Oct. 25, 2002; U.S. patent application Ser. No. 10/323,390, filed on Dec. 19, 2002; U.S. patent application Ser. No. 10/323,513, filed on Dec. 19, 2002; U.S. patent application Ser. No. 10/323,389, filed on Dec. 19, 2002; U.S. patent application Ser. No. 10/323,388, filed on Dec. 19, 2002; U.S. patent application Ser. No. 10/340,942, filed on Jan. 13, 2003; International Patent Application No. PCT/US12/51265, filed on Aug. 17, 2012; U.S. patent application Ser. No. 13/921,311, filed on Jun. 19, 2013; and U.S. patent application Ser. No. 14/222,841, filed on Mar. 24, 2014; all of which are hereby incorporated by reference in their entireties.

With these structures, a fabrication sequence can be used to make the devices on a common substrate. In other words, n type and p type contacts, critical etches, etc. can be used to realize all of these devices simultaneously on a common substrate. The essential features of this device structure include 1) an n-type modulation doped quantum well interface and a p-type modulation doped quantum well interface, 2) self-aligned n-type and p-type channel contacts formed by ion implantation, 3) n-type metal contacts to the n-type ion implants and the bottom n-type layer structure, and 4) p-type metal contacts to the p-type ion implants and the top p-type layer structure. The active device structures can be realized with group III-V materials. Such group III-V materials can include gallium (Ga) and arsenic (As) (for gallium arsenide layer structures) as well as aluminum (Al) and indium (In), and thus can include GaAs, AlGaAs, and InGaAs semiconductor alloys. Alternatively, such group III-V materials can include gallium (Ga) and nitrogen (N) (for gallium nitride layer structures) as well as aluminum (Al) and indium (In), and thus can include GaN, AlGaN, and InGaN semiconductor alloys.

POET can be used to construct a variety of optoelectronic devices. POET can also be used to construct a variety of high performance transistor devices, such as complementary n-channel and p-channel HFET unipolar transistor devices as well as n-type and p-type HBT bipolar transistor devices.

Turning now to FIG. **17**, the device structure of the present application includes an optional bottom dielectric distributed Bragg reflector (DBR) mirror **1703** formed on substrate **1701**. The bottom DBR mirror **1703** can be formed by depositing pairs of semiconductor or dielectric materials with different refractive indices. When two materials with different refractive indices are placed together to form a junction, light will be reflected at the junction. The amount of light reflected at one such boundary is small. However, if multiple junctions/layer pairs are stacked periodically with each layer having a quarter-wave ($\lambda/4$) optical thickness, the reflections from each of the boundaries will be added in phase to produce a large amount of reflected light (e.g., a large reflection coefficient) at the particular center wavelength λ_C. Deposited upon the bottom DBR mirror **1703** or upon the substrate **1701** for the case where the bottom DBR mirror **1703** is omitted) is the active device structure suitable for realizing complementary heterostructure field-effect transistor (HFET) devices. The first of these complementary HFET devices is a p-channel HFET formed from a p-type modulation doped quantum well (QW) structure **1711** with an n-type gate region (i.e., n-type ohmic contact layer **1705** and n-type layer(s) **1707**) below the p-type modulation doped QW structure **1711**. An undoped spacer layer **1709** is disposed between the p-type modulation doped quantum well (QW) structure **1711** and the underlying n-type layer(s) **1707**. One or more spacer layers **1713** are disposed above the p-type modulation doped QW structure **1711**. The second of these complementary HFET devices is an n-channel HFET formed by an n-type modulation doped QW structure **1715** with a p-type gate region (i.e., p-type layer(s) **1719** and p-type ohmic contact **1721**) disposed above the n-type modulation doped QW structure **1715**. An undoped spacer layer **1717** is disposed between the n-type modulation doped QW structure **1715** and the overlying p-type layer(s) **1719**. The layers encompassing the spacer layer **1713** and the n-type modulation doped QW structure **1715** forms the collector region of the p-channel HFET. Similarly, the layers encompassing the spacer layer **1713** and the p-type modulation doped QW structure **1711** forms the collector region of the n-channel HFET. Such collector regions are analogous to the substrate region of a MOSFET device as is well known. Therefore, a non-inverted re-channel HFET device can be stacked upon an inverted p-channel HFET device as part of the active device structure.

The active device layer structure begins with n-type ohmic contact layer(s) **1705** which enables the formation of ohmic contacts thereto. Deposited on layer **1705** are one or more n-type layers **1707** and an undoped spacer layer **1709** which serve electrically as part of the gate of the p-channel HFET device and optically as a part of the lower waveguide cladding of the active device structure. Deposited on layer **17089** is the p-type modulation doped QW structure **1711** that defines a p-type charge sheet offset from one or more QWs (which may be formed from strained or unstrained heterojunction materials) by an undoped spacer layer. The p-type charge sheet is

formed first below the undoped spacer and the one or more QWs of the p-type modulation doped QW structure **1711**. All of the layers grown thus far form the p-channel HFET device with the gate ohmic contact on the bottom. Deposited on the p-type modulation doped QW structure **1711** is one or more spacer layers **1713**.

Deposited on the spacer layer(s) **1713** is the n-type modulation doped QW structure **1715**. The n-type modulation doped QW structure **1715** defines an n-type charge sheet offset from one or more QWs by an undoped spacer layer. The n-type charge sheet is formed last above the undoped spacer and the one or more QWs of the n-type modulation doped QW structure **1715**.

Deposited on the n-type modulation doped QW structure **1715** is an undoped spacer layer **1717** and one or more p-type layers **1719** which can serve electrically as part of the gate of the n-channel HFET and optically as part of the upper waveguide cladding of the device. The p-type layers **1719** can include two sheets of planar doping of highly doped p-material separated by a lightly doped layer of p-material. These p-type layers are offset from the n-type modulation doped quantum well structure **1715** by the undoped spacer layer **1717**. In this configuration, the top charge sheet achieves low gate contact resistance and the bottom charge sheet defines the capacitance of the n-channel HFET with respect to the n-type modulation doped QW structure **1715**. Deposited on p-type layer(s) **1719** is one or more p-type ohmic contact layer(s) **1721**, which enables the formation of ohmic contacts thereto.

For the n-channel HFET device, a gate terminal electrode of the n-channel HFET device interfaces to the top p-type ohmic contact layer(s) **1721**. A source terminal electrode and a drain terminal electrode of the n-channel HFET device are operably coupled to opposite sides of a QW channel region realized in the n-type modulation doped QW structure **1715**. One or more collector terminal electrodes can be operably coupled to the p-type modulation doped QW structure **1711**.

For the p-channel HFET device, a gate terminal electrode of the p-channel HFET device interfaces to the bottom n-type ohmic contact layer **1705**. A source terminal electrode and a drain terminal electrode are operably coupled to opposite sides of a QW channel region realized in the p-type modulation doped QW structure **1711**. The layer structure of the p-channel HFET device can be patterned and etched down to form a mesa at spacer layer **1713** with a collector (or back-gate) electrode formed on such mesa.

It may be beneficial that the depth of the back-gate mesa be uniform for the p-channel HFET devices formed on the substrate. Attempting to achieve this uniform depth by timed etching is difficult due to etch non-uniformity and thermal variations. A solution can be found by introducing an extremely thin layer (e.g. **10**A) of AlAs during the epitaxial growth at the level of the back-gate mesa of the p-channel HFET devices. This AlAs layer can act as an etch stop layer during etching in order to provide a uniform depth for the back-gate mesas of the p-channel HFET devices formed on the substrate. In one embodiment, a dry etch can be performed to above and within **600**A of the thin AlAs layer. Then a wet etch (preferably employing citric acid and H_2O_2 can be performed. This etch process stops naturally at the AlAs layer (i.e., the AlAs of **10**A is extremely resistant to this etching process). Thus a planar surface is established just at the back gate level which has the accuracy of the MBE growth.

Both the n-channel HFET device and the p-channel HFET device are field effect transistors where current flows as a two-dimensional gas through the QW channel region with contacts on either side of the channel region. The basic transistor action is the modulation of the QW channel conductance by a modulated electric field that is perpendicular to the QW channel. The modulated electric field modulates the QW channel conductance by controlling an inversion layer (i.e., a two-dimensional electron gas for the n-channel HFET device or a two-dimensional hole gas for the p-channel HFET) as a function of gate voltage relative to source voltage.

For the n-channel HFET device, the QW channel conductance is turned on by biasing the gate terminal electrode and the source terminal electrode at voltages where the P/N junction of the gate and source regions is forward biased with minimal gate conduction and an inversion layer of electron gas is created in the QW channel of the n-type modulation doped quantum well structure **1715** between the source terminal electrode and the drain terminal electrode. In this configuration, the source terminal electrode is the terminal electrode from which the electron carriers enter the QW channel of the n-type modulation doped quantum well structure **1715**, the drain terminal electrode is the terminal electrode where the electron carriers leave the device, and the gate terminal electrode is the control terminal for the device.

The p-channel HFET device operates in a similar manner to the n-channel HFET device with the current direction and voltage polarities reversed with respect to those of the n-channel HFET device. For the p-channel HFET device, the QW channel conductance is turned on by biasing the gate terminal electrode and the source terminal electrode at a voltage where the P/N junction of the source and gate regions is forward-biased with minimal gate conduction and an inversion layer of hole gas is created in the QW channel of the p-type modulation doped quantum well structure **1711** between the source terminal electrode and the drain terminal electrode. In this configuration, the source terminal electrode is the terminal from which the hole carriers enter the QW channel of the p-type modulation doped quantum well structure **1711**, the drain terminal electrode is the terminal where the hole carriers leave the device, and the gate terminal electrode is the control terminal for the device.

The device structure of the present application can also be configured to realize bipolar inversion channel field-effect transistors (BICFETs) with either an n-type modulation doped quantum well inversion channel base region (n-channel base BICFET) or a p-type modulation doped quantum well inversion channel base region (p-channel base BICFET).

For the n-channel base BICFET device, an emitter terminal electrode of the n-channel base BICFET device interfaces to the top p-type ohmic contact layer(s) **1721** of the active device structure. A base terminal electrode of the n-channel base BICFET device is operably coupled to the QW channel region realized in the n-type modulation doped QW structure **1715**. A collector terminal electrode of the n-channel base BICFET device is operably coupled to the p-type modulation doped QW structure **1711**. The n-channel base BICFET device is a bipolar junction type transistor which can be operated in an active mode by applying a forward bias to the PN junction of the emitter and base regions while applying a reverse bias to the PN junction of the base and collector regions, which causes holes to be injected from the emitter terminal electrode to the collector terminal electrode. Because the holes are positive carriers, their injection contributes to current flowing out of the collector terminal electrode as well as current flowing into the emitter terminal electrode. The bias conditions also cause electrons to be injected from the base to the emitter, which contributes to current flowing out of the base terminal electrode as well as the current flowing into the emitter terminal electrode.

The p-channel base BICFET device is similar in construction to the p-channel HFET device with the following adaptations. An emitter terminal electrode of the p-channel base BICFET device, which is analogous to the gate terminal electrode of the p-channel HFET device, interfaces to the bottom n-type ohmic contact layer(s) **1721** of the active device structure. A base terminal electrode of the p-channel base BICFET device, which is analogous to the source or drain electrode of the p-channel HFET device, is operably coupled to the QW channel region realized in the p-type modulation doped QW structure **1711**. A collector terminal electrode of the p-channel base BICFET device, which is analogous to the collector terminal electrode of the p-channel HFET device, is operably coupled to the spacer layer **1713**. The p-channel base BICFET device is a bipolar junction type transistor which can be operated in an active mode by applying a forward bias to the PN junction of the emitter and base regions while applying a reverse bias to the PN junction of the base and collector regions, which causes electrons to be injected from the emitter terminal electrode to the collector terminal electrode. Because the electrons are negative carriers, their injection contributes to current flowing into the collector terminal electrode as well as current flowing out of the emitter terminal electrode. The bias conditions also cause holes to be injected from the base to the emitter, which contributes to current flowing into the base terminal electrode as well as the current flowing out of the emitter terminal electrode.

The active device structure of the present application can also be configured to realize a variety of electrical and optoelectronic thyristor devices having a vertical P-N-P-N thyristor structure. The upper p-type region (i.e., the first P) of the vertical P-N-P-N thyristor structure is formed by the p-type layers **1719**, **1721** of the active device structure. The upper n-type region (i.e., the first N) of the vertical P-N-P-N thyristor structure is formed from the n-type modulation doped QW structure **1715** of the active device structure. The lower p-type region (i.e., the second P) of the vertical P-N-P-N thyristor structure is formed from the p-type modulation doped QW structure **1711** of the active device structure. The lower n-type region (i.e., the second N) of the vertical P-N-P-N thyristor structure is formed by the bottom n-type layers **1705**, **1707** of the active device structure.

180-Degree Optical Hybrid Coupler

FIGS. **18**A-**18**C illustrate a configuration of a 180-degree optical hybrid coupler that can be made utilizing the layer structure of FIG. **17**, which includes two zig-zag active waveguide structures **1801**, **1803** integrated on the substrate **1701** and optically coupled to one another by evanescent-wave coupling over a gap region G. The zig-zag waveguide structure **1801** is defined by a rib waveguide **1805** that forms a zig-zag path. Similarly, the zig-zag waveguide structure **1803** is defined by a rib waveguide **1807** that forms a zig-zag path. The optical mode that travels through each respective rib waveguide is strongly confined within the respective rib waveguide by internal reflection at the reflective interfaces of the rib waveguide. Specifically, cladding for guiding the optical mode **1809** in the rib waveguide **1807** is provided by the top DBR mirror **1830** and the bottom DBR mirror **1703** as best shown in the cross-section of FIG. **18**B. Lateral confinement of the optical mode **1809** in the waveguide **1807** is provided by refractive index changes at the sidewalls **1811**, **1813** that define the outer boundary of the waveguide **18007** (FIGS. **18**A and **18**B), at n-type ion implants **1816** adjacent the top rib sidewalls **1811**, **1813** (FIG. **18**B), at the corner sidewalls, and at the interface of the top mirror **1830** that covers the waveguide **1807**. Similar structure is used guiding the optical mode **1815** in the rib waveguide **1805**.

In the coupling region, the waveguides **1805** and **1807** include straight sections that extend parallel to one another and closely-spaced from one another by the gap region G. In the straight section of the waveguide **1805**, vertical confinement of the optical modes **1815**, **1809** in the waveguides **1805**, **1807** can be aided by the top mirror **1830** formed to cover the top and sidewalls of the waveguides **1805**, **1807** as shown. Lateral confinement of the optical mode **1815** is provided by i) a refractive index change at the periphery of the implant region **1817** under the metal of the top control electrode **1819** as shown in FIG. **18**C, and ii) a refractive index change at the periphery of the implant region **1821** in the coupling region (gap G) as evident from FIG. **18**C. In the straight section of the waveguide **1807**, lateral confinement of the optical mode **1809** is provided by i) a refractive index change at the periphery of the implant region **1823** under the metal of the top control electrode **1825** as shown in FIG. **18**C, and ii) a refractive index change at the periphery of the implant region **1821** in the coupling region (gap G) as evident from FIG. **18**C.

The width (W) of the waveguides **1805**, **1807** can be less than 2 μm, and possibly 1 μm or less. The width of the gap region G (i.e., the spacing between the waveguides **1805**, **1807**) can be less than 2 μm, and possibly on the order of 1 μm or less.

The zig-zag active waveguide structure **1801** includes the top control terminal electrode **1819** that is electrically coupled to the top p-type ohmic contact layer **1107**, a second control terminal electrode **1827** that is electrically coupled to the n-type modulation doped QW structure **1715** via an n-type ion implant **1816**, and a bottom electrode **1829** that is electrically coupled to the bottom n-type contact layer **1705** as best shown in FIG. **18**C.

The zig-zag active waveguide structure **1803** includes a top control terminal electrode **1825** that is electrically coupled to the top p-type ohmic contact layer **1107**, a second control terminal electrode **1831** that is electrically coupled to the n-type modulation doped QW structure **1715** via an n-type ion implant **1816**, and a bottom electrode **1833** that is electrically coupled to the bottom n-type contact layer **1705** as best shown in FIG. **18**C. Note that the implant regions **1817**, **1821**, **1823** can locally shift the band gap in the underlying n-type modulation doped quantum well structure **1715**. This bandgap shift can prohibit charge transfer in the QWs of the n-type modulation doped QW structure **1715** across the gap region G between the adjacent waveguides **1805**, **1807**. For the waveguide **1805**, voltage signals applied to the top control electrode **1819** can overcome this effect to allow charge to enter (or exit) from the QWs of the n-type modulation doped QW structure **1715** via the corresponding second control electrode **1827** as desired. For the waveguide **1807**, voltage signals applied to the top control electrode **1525** can overcome this effect to allow charge to enter (or exit) from the QWs of the n-type modulation doped QW structure **1715** via the corresponding second control electrode **1831** as desired. It is also contemplated that additional process steps, such as etching away the top p+ contact layers **1721** and possibly additional layers thereunder in the gap region G between the adjacent waveguides **1805** and **1807** can be performed in order to prevent any charge transfer across the gap region G between the adjacent waveguides **1805** and **1807**.

The 180-degree hybrid coupler of FIGS. **18**A to **18**C includes two input waveguides (In0/In1) and two output waveguides (Out0/Out1). The input waveguide In0 is defined by one end of the waveguide **1805**. The output waveguide

Out0 is defined by the other end of the zig-zag waveguide **1805**. The input waveguide In1 is defined by one end of the waveguide **1807**. The output waveguide Out0 is defined by the other end of the zig-zag waveguide **1807**. The two input waveguides In0, In1 receive two separate input optical signals S**0** and S**1** as shown. The length of the coupling region of the two waveguides **1805** and **1807** (i.e., the straight sections that extend parallel to one another and closely-spaced from one another by the gap region G) is configured such that the evanescent coupling over the coupling region of the two waveguides **1805** and **1807** mixes the two input optical signals S**0** and S**1** to produce two output signals that propagate out from the Out0 and Out1 waveguides where the power of the two input optical signals S**0**, S**1** is split evenly (50:50 split for each input signal) in each one of two output signals.

The power transfer ratio between the two input waveguides (In0/In1) may be written as a function of $\Delta\beta$, which is the propagation constant difference due to the phase mismatch introduced by the charge difference in the two waveguides. The equation is given as:

$$T = \left(\frac{\pi}{2}\right)^2 \mathrm{sinc}^2\left\{\frac{1}{2}\left[1+\left(\frac{\Delta\beta L_o}{\pi}\right)^2\right]^{1/2}\right\} \quad (11)$$

where $L_o=\pi/2\zeta$ is the fixed coupling length, and ζ is the coupling coefficient.

For $\Delta\beta=0$, 100% power is transferred in L_o, and for $\Delta\beta L_o=\sqrt{3}\pi$ there is no power transferred. For a 50:50 split where the power of the two input optical signals S**0**, S**1** is split evenly in each one of two output signals, the values of $\Delta\beta$ would be used for a fixed L_o according to Eqn. (11).

The structures of FIGS. **18**A-**18**C can also be adapted to provide the specific phase modulators as described above $\pi/4$ for FIGS. **7**A and **9**A, and $3\pi/8$ for FIG. **9**A. The phase modulator is the simplest of devices. A straight waveguide is injected along one or both sides with charge to produce $\Delta\beta$ which corresponds to the desired phase change upon propagating a distance L_o, which is selected according to Eqn. (11) above.

NHFET Phototransistor

FIGS. **19**A and **19**B show an exemplary embodiment of an n-channel HFET (NHFET) phototransistor device **1900**. A straight passive rib waveguide section **1901** operates to passively guide light (optical mode **1903** of FIG. **19**B) into the active waveguide region of the n-channel HFET phototransistor device **1900**. The straight passive rib waveguide section **1901** can employ a top DBR mirror (labeled as **1930** in FIG. **19**B), which can be realized by pairs of semiconductor or dielectric materials with different refractive indices) that operates as cladding to provide guiding of the optical mode **1903** between the top DBR mirror and the bottom DBR mirror **1703** formed on the substrate **1701**. The lateral confinement of the optical mode **1903** within the passive rib waveguide section **1901** can be provided by the index change associated with vertical sidewalls **1902** of the passive rib waveguide section **1901** and possibly n-type ion implants in the top layers **1721**, **1719**, **1717** (labeled as **1905** in FIG. **19**B). The n-type implants of the passive rib waveguide section **1901** can introduce impurity free vacancy disordering into the adjacent waveguide core region when subjected to rapid thermal annealing. The bandgap of the disordered waveguide core region is increased locally to substantially reduce absorption and associated optical loss. The lateral confinement of the optical mode **1903** can also be supported by covering the sidewalls **1902** with the top DBR mirror. The top DBR mirror structure can also extend in a continuous manner to form cladding over the active waveguide region of the n-channel HFET phototransistor device **1900** as is evident from the cross-section of FIG. **19**B. In this configuration, the top DBR mirror structure **1930** operates as cladding for the optical mode **1903** received by the active waveguide region of the n-channel HFET phototransistor device **1900**.

The active waveguide region of the n-channel HFET phototransistor device **1900** is defined by a rib waveguide formed in the top layers **1721**, **1719**, **1717** that is aligned (both vertically and laterally) with the passive rib waveguide section **1901** as evident from FIG. **19**A. The lateral confinement of the optical mode **1903** within the active waveguide region of the n-channel HFET phototransistor device **1900** can be provided by the index change associated with vertical sidewalls **1907** of the rib formed in the top layers **1721**, **1719**, **1717** and possibly n-type ion implants **1905** in the top p-type layers **1721**, **1719**, **1717** as shown in FIG. **19**B. The n-type implants **1905** can introduce impurity free vacancy disordering into the adjacent waveguide core region when subjected to rapid thermal annealing. The bandgap of the disordered waveguide core region is increased locally to substantially reduce absorption and associated optical loss. The lateral confinement of the optical mode **1903** can also be supported by covering the sidewalls **1907** with the top DBR mirror **1230**.

A source terminal electrode and a drain terminal electrode are operably coupled to opposite sides of an elongate QW channel(s) realized in the n-type modulation doped QW structure **1715** of the active waveguide region of the n-channel HFET phototransistor device **1900**. A collector terminal electrode can be coupled to the p-type modulation doped QW structure **1711** of the active waveguide region of n-channel HFET phototransistor device **1900**.

Specifically, the layer structure of the n-channel HFET phototransistor device **1900** is patterned and etched to form the rib of the active waveguide region that extends to opposed elongate intermediate mesas **1909**, **1911** in the spacer layer **1717** above the n-type modulation doped QW structure **1715**. The layer structure is also patterned and etched to form a vertical sidewall **1913** that defines the end of the active waveguide region of the n-channel HFET phototransistor device **1900** opposite the passive rib waveguide section **1901**. The vertical sidewall **1913** extends down to an elongate intermediate mesa **1915** in the spacer layer **1713** above the p-type modulation doped QW structure **1711**.

N-type donor ions can be implanted through the mesas **1909**, **1911** to form n-type ion implant regions **1917** that create the self-aligned n-type contacts to the n-type modulation doped quantum well structure **1715** that forms the QW channel(s) of the active waveguide region of the n-channel HFET phototransistor device **1900**. P-type donor ions can be implanted through the mesa **1915** to form a p-type ion implant region that creates a self-aligned p-type contact to the p-type modulation doped quantum well structure **1711** of the active waveguide region of the n-channel HFET phototransistor device **1900**. Deposition of a rapid thermal anneal (RTA) oxide and subsequent RTA operations can be carried out to activate the implant regions.

The metal that defines the Source and Drain terminal electrodes is deposited and patterned on the mesas **1909** and **1911** in contact with the n-type ion implant regions **1917** in order to contact the n-type modulation doped quantum well structure **1715** that forms the QW channel(s) of the active waveguide region of the re-channel HFET phototransistor device **1900**. The metal that defines the Collector terminal electrode, is deposited and patterned on the mesa **1915** in contact with the p-type ion implant region in order to contact the p-type modu-

lation doped quantum well structure of the active waveguide region of the n-channel HFET phototransistor device **1900**. The resultant structure can be heated to treat the metals of the source, drain and collector electrodes as desired.

The n-channel HFET phototransistor device **1900** is a field effect transistor where current flows as a two-dimensional gas through the QW channel region of the n-type modulation doped quantum well structure **1715** of the active waveguide region with the Source and Drain terminals on either side of the QW channel region. The basic transistor action is the modulation of the QW channel conductance by an inversion layer (i.e., a two-dimensional electron gas) that is produced by the absorption of the optical mode **1903** propagating within the active waveguide region of the n-channel HFET phototransistor device **1900**. Specifically, the QW channel conductance is controlled by the absorption of the optical mode **1903** propagating within the active waveguide region of the n-channel HFET phototransistor device **1900**, which produces an inversion layer of electron gas in the QW channel of the n-type modulation doped quantum well structure **1715** between the Source terminal electrode and the Drain terminal electrode. In this configuration, the Source terminal electrode is the terminal electrode from which the electron carriers enter the QW channel of the n-type modulation doped quantum well structure **1715**, and the Drain terminal electrode is the terminal electrode where the electron carriers leave the device.

PHFET Phototransistor

FIGS. **20**A and **20**B show an exemplary embodiment of a p-channel HFET (PHFET) phototransistor device **2000**. A straight passive rib waveguide section **2001** operates to passively guide light (optical mode **2003** of FIG. **20**B) into the active waveguide region of the p-channel HFET phototransistor device **2000**. The straight passive rib waveguide section **2001** can employ a top DBR mirror (labeled as **2030** in FIG. **20**B), which can be realized by pairs of semiconductor or dielectric materials with different refractive indices) that operates as cladding to provide guiding of the optical mode **2003** between the top DBR mirror and the bottom DBR mirror **1703** formed on the substrate **1701**. The lateral confinement of the optical mode **2003** within the passive rib waveguide section **2001** can be provided by the index change associated with vertical sidewalls **2002** of the passive rib waveguide section **2001** and possibly n-type ion implants in the top layers **1721**, **1719**, **1717** (labeled as **2005** in FIG. **19**B). The n-type implants of the passive rib waveguide section **2001** can introduce impurity free vacancy disordering into the adjacent waveguide core region when subjected to rapid thermal annealing. The bandgap of the disordered waveguide core region is increased locally to substantially reduce absorption and associated optical loss. The lateral confinement of the optical mode **2003** can also be supported by covering the sidewalls **2002** with the top DBR mirror. The top DBR mirror structure can also extend in a continuous manner to form cladding over the active waveguide region of the p-channel HFET phototransistor device **2000** as is evident from the cross-section of FIG. **20**B. In this configuration, the top DBR mirror structure **2030** operates as cladding for the optical mode **2003** received by the active waveguide region of the p-channel HFET phototransistor device **2000**.

The active waveguide region of the p-channel HFET phototransistor device **2000** is defined by a rib waveguide formed in layers **1721**, **1719**, **1717**, **1715**, and **1713** that is aligned (both vertically and laterally) with the passive rib waveguide section **2001** as evident from FIG. **20**A. The lateral confinement of the optical mode **2003** within the active waveguide region of the p-channel HFET phototransistor device **2000** can be provided by the index change associated with vertical sidewalls **2007** of the rib formed in the layers **1721**, **1719**, **1717**, **1715**, and **1713** and possibly n-type ion implants **2005** in the top p-type layers **1721**, **1719**, **1717** as shown in FIG. **20**B. The n-type implants **2005** can introduce impurity free vacancy disordering into the adjacent waveguide core region when subjected to rapid thermal annealing. The bandgap of the disordered waveguide core region is increased locally to substantially reduce absorption and associated optical loss. The lateral confinement of the optical mode **2003** can also be supported by covering the sidewalls **2007** with the top DBR mirror **2030**.

A source terminal electrode and a drain terminal electrode are operably coupled to opposite sides of an elongate QW channel(s) realized in the p-type modulation doped QW structure **171** of the active waveguide region of the p-channel HFET phototransistor device **2000**. A collector terminal electrode can be coupled to the n-type modulation doped QW structure **1715** of the active waveguide region of p-channel HFET phototransistor device **2000**.

Specifically, the layer structure of the p-channel HFET phototransistor device **2000** is patterned and etched to form the rib of the active waveguide region that extends to opposed elongate intermediate mesas **2009**, **2011** in the spacer layer **1713** above the p-type modulation doped QW structure **1711**. The layer structure is also patterned and etched to form a vertical sidewall **2013** that defines the end of the active waveguide region of the p-channel HFET phototransistor device **2000** opposite the passive rib waveguide section **2001**. The vertical sidewall **2013** extends down to an elongate intermediate mesa **2015** in the spacer layer **1717** above the n-type modulation doped QW structure **1715**.

P-type donor ions can be implanted through the mesas **2009**, **2011** to form p-type ion implant regions **2017** that create the self-aligned p-type contacts to the p-type modulation doped quantum well structure **1711** that forms the QW channel(s) of the active waveguide region of the p-channel HFET phototransistor device **2000**. N-type donor ions can be implanted through the mesa **2015** to form an n-type ion implant region that creates a self-aligned n-type contact to the n-type modulation doped quantum well structure **1715** of the active waveguide region of the p-channel HFET phototransistor device **2000**. Deposition of a rapid thermal anneal (RTA) oxide and subsequent RTA operations can be carried out to activate the implant regions.

The metal that defines the Source and Drain terminal electrodes is deposited and patterned on the mesas **2009** and **2011** in contact with the p-type ion implant regions **2017** in order to contact the p-type modulation doped quantum well structure **1711** that forms the QW channel(s) of the active waveguide region of the p-channel HFET phototransistor device **2000**. The metal that defines the Collector terminal electrode, is deposited and patterned on the mesa **2015** in contact with the n-type ion implant region in order to contact the n-type modulation doped quantum well structure of the active waveguide region of the p-channel HFET phototransistor device **2000**. The resultant structure can be heated to treat the metals of the source, drain and collector electrodes as desired.

The p-channel HFET phototransistor device **2000** is a field effect transistor where current flows as a two-dimensional gas through the QW channel region of the p-type modulation doped quantum well structure **1711** of the active waveguide region with the Source and Drain terminals on either side of the QW channel region. The basic transistor action is the modulation of the QW channel conductance by an inversion layer (i.e., a two-dimensional hole gas) that is produced by the absorption of the optical mode **2003** propagating within the

active waveguide region of the p-channel HFET phototransistor device **2000**. Specifically, the QW channel conductance is controlled by the absorption of the optical mode **2003** propagating within the active waveguide region of the p-channel HFET phototransistor device **2000**, which produces an inversion layer of hole gas in the QW channel of the p-type modulation doped quantum well structure **1711** between the Source terminal electrode and the Drain terminal electrode. In this configuration, the Source terminal electrode is the terminal from which the hole carriers enter the QW channel of the p-type modulation doped quantum well structure **1711**, and the drain terminal electrode is the terminal where the hole carriers leave the device.

Note that the n-channel and p-channel HFET phototransistors will have similar optical responses since the absorption characteristics are similar and the transmission of both holes and electrons is required in both. In the n-channel HFET phototransistor, the optical mode will be guided by both sets of quantum wells; whereas, in the p-channel n-channel HFET phototransistor, the top quantum well will be removed so only the bottom quantum well will provide guidance of the optical mode. One difference is the polarity of voltage required for operation. The n-channel HFET phototransistor operates with a positive drain-source voltage so that the Source terminal electrode of the n-channel HFET phototransistor may be grounded and the light increases the channel current flowing from a positive circuit node to ground. In contrast, the p-channel HFET phototransistor operates with a negative drain-source voltage so that the Source terminal electrode of the p-channel HFET phototransistor may be electrically coupled to a positive supply voltage and the absorbed light increases the current flowing from the fixed positive rail voltage to a less positive circuit node. Because of this difference in reference voltages, the n-channel and p-channel HFET phototransistors are ideal for steering photocurrent either into or out of an intermediate circuit node which operates at voltages between the positive and negative supply voltages (such as the re-channel injector terminal or p-channel injector terminal of a thyristor as described herein). This is the configuration of the coherent balanced receiver.

The n-channel and p-channel HFET phototransistors have advantages over a simple diode detector. More specifically, a diode detector produces photocurrent characterized by low current (high resistance) and high capacitance. Therefore, a transimpedance amplifier is necessary to amplify the output of the diode detector in order to increase the bandwidth. However, the n-channel and p-channel HFET phototransistors have an internal transconductance (g_m=dV/dI) and hence produces voltage output directly without the need for a transimpedance amplifier.

Thyristor-Based Optoelectronic Oscillator

FIGS. **21**A-**21**D show an embodiment of an optical thyristor **2100** formed from the epitaxial device structure of FIG. **17** that can be configured for use as the optoelectronic oscillator. The optical thyristor **2100** includes a thyristor closed-path waveguide resonator **2101** spaced from a section of a first zig-zag waveguide structure **2109**A by a gap region **2113**A as shown in FIGS. **21**A and **21**B. The first zig-zag waveguide structure **2109**A is optically coupled to the resonator **2101** by evanescent-wave coupling over the gap region **2113**A. The optical thyristor **2100** can also include an optional second zig-zag waveguide structure **2109**B that is spaced from the thyristor closed-path waveguide resonator **2101** by a gap region **2113**B. The second zig-zag waveguide structure **2109**B is optically coupled to the resonator **2101** by evanescent-wave coupling over the gap region **2113**B.

The resonator **2101** defines a resonant cavity waveguide **2102** that follows a closed path that is generally rectangular in shape. The optical path length of the resonant cavity waveguide **2102** is tuned to the particular wavelength of the optical mode signal that is to propagate in the resonant cavity waveguide **2102**. Specifically, the length of the rectangular closed path of the resonant cavity waveguide **2102** is given as $2(L_1+L_2)$ and the L_1 and L_2 parameters are selected to conform to the following:

$$2(L_1 + L_2) = \frac{2\pi m\lambda_c}{n_{eff}} \tag{12}$$

where

L_1 and L_2 are the effective lengths of the opposed sides of the active resonant cavity waveguide **2102**;

m is an integer greater than zero;

λ_C is the center wavelength of the optical mode that is to propagate in the resonant cavity waveguide **2102**; and

n_{eff} is the effective refractive index of the resonant cavity waveguide **2102**.

The width (W) of the resonant cavity waveguide **2102** can be less than 2 μm, and possibly 1 μm or less. The width of the gap region **2113**A (i.e., the spacing between the resonant cavity waveguide **2102** and the zig-zag waveguide **2109**A) can be less than 2 μm, and possibly on the order of lμm or less. The width of the gap region **2113**B (i.e., the spacing between the resonant cavity waveguide **2102** and the zig-zag waveguide **2109**B) can be less than 2 μm, and possibly on the order of 1 μm or less.

The optical mode circulates around the resonant cavity waveguide **2102** and is strongly confined within the resonant cavity waveguide **2102** by internal reflection at the reflective interfaces of the resonant cavity waveguide **2102**. The zig-zag waveguide **2109**A defines a passive rib waveguide that forms a zig-zag path. The optical mode is strongly confined within the zig-zag waveguide **2109**A by internal reflection at the reflective interfaces of the zig-zag waveguide **2109**A. The zig-zag waveguide **2109**B defines a passive rib waveguide that forms a zig-zag path. The optical mode is strongly confined within the zig-zag waveguide **2109**B by internal reflection at the reflective interfaces of the zig-zag waveguide **2109**B.

The resonant cavity waveguide **2102** can be logically partitioned in four sections that are coupled to one another by corners as shown in FIG. **21**A. The four sections include a straight section that extends parallel to and is closely-spaced from a straight section of the first zig-zag waveguide **2109**A by the gap region **313**A. This straight section is configured to provide evanescent coupling to (or from) the straight section of the zig-zag waveguide **2109**A for the optical mode signal that circulates in the resonant cavity waveguide **2102**. The opposed straight section is configured to provide evanescent coupling to (or from) the straight section of the zig-zag waveguide **2109**B for the optical mode signal that circulates in the resonant cavity waveguide **2102**. All four sections of the resonant cavity waveguide **2102** are configured as active portions that contribute to the detection (and possibly generation) of the optical mode signal that circulates in the resonant cavity waveguide **2102**. Such active portions can be configured with mesas, contact implants and metallization for operation as a switching optical thyristor.

In this configuration, the mesas, contact implants and metallization provide electrical contact to the top p-type ohmic contact layer **1721** for the anode terminal electrode (or parts

thereof) of the optical thyristor as well as electrical contact to the n-type modulation doped QW structure **1715** for an n-channel injector terminal electrode or parts thereof of the optical thyristor as well as electrical contact to the p-type modulation doped QW structure **1171** for a p-channel injector terminal electrode or parts thereof of the optical thyristor as well as electrical contact to the bottom n-type contact layer **1705** for a cathode terminal electrode or parts thereof of the optical thyristor.

The zig-zag waveguide **2109**A that extends along the gap region **2113**A can be configured with mesas, contact implants and metallization for electrical contact to top p-type ohmic contact layer **1721** for a first coupling control terminal electrode **2115**A as well as electrical contact to the n-type modulation doped QW structure **1715** for a second control electrode **2117**A that are used to control the coupling coefficient of the evanescent-wave coupling between the resonant cavity waveguide **2102** and the zig-zag waveguide **2109**A. Bias circuitry (not shown) can be configured to control the coupling coefficient of the evanescent-wave coupling. Specifically, the coupling coefficient of the evanescent-wave coupling between two waveguides can be changed (i.e., modulated) by controlling the amount of charge (electrons) that fills the QW(s) of the n-type modulation doped QW structure **1715** for the straight section of the resonant cavity waveguide **2102** that extends along the gap region **2113**A, which dictates the shifting of the absorption edge and index of refraction of the QW(s) of the n-type modulation doped QW structure **1715** for this straight section of the resonant cavity waveguide **2102**. The bias circuitry can be realized by suitable transistor circuitry that can be integrally formed on the substrate of the integrated circuit.

The zig-zag waveguide **2109**B that extends along the gap region **2113**B can be configured with mesas, contact implants and metallization for electrical contact to top p-type ohmic contact layer **1721** for a first coupling control terminal electrode **2115**B as well as electrical contact to the n-type modulation doped QW structure **1715** for a second control electrode **2117**B (not shown in FIG. **21**A) that are used to control the coupling coefficient of the evanescent-wave coupling between the resonant cavity waveguide **2102** and the zig-zag waveguide **2109**B. Bias circuitry (not shown) can be configured to control the coupling coefficient of the evanescent-wave coupling. Specifically, the coupling coefficient of the evanescent-wave coupling between two waveguides can be changed (i.e., modulated) by controlling the amount of charge (electrons) that fills the QW(s) of the n-type modulation doped QW structure **1715** for the straight section of the resonant cavity waveguide **2102** that extends along the gap region **2113**B, which dictates the shifting of the absorption edge and index of refraction of the QW(s) of the n-type modulation doped QW structure **1715** for this straight section of the resonant cavity waveguide **2102**. The bias circuitry can be realized by suitable transistor circuitry that can be integrally formed on the substrate of the integrated circuit.

As shown in FIG. **21**C, the optical mode signal **2104** that circulates around the waveguide **2102** is strongly confined within the waveguide **2102** by internal reflection at the reflective interfaces of the waveguide **2102**. Specifically, cladding for guiding the optical mode **2104** in the waveguide **2102** can be provided by a top DBR mirror structure (not shown) and the bottom DBR mirror **1703**. Lateral confinement of the optical mode **2104** in the waveguide **2102** can be provided by: i) a refractive index change at the sidewalls that define the outer boundary of the waveguide **2102**, ii) a refractive index change at the periphery of n-type contact implant regions **2121** under the n-channel injector electrode parts located adjacent the sidewalls of the rib waveguide **2012**, iii) a refractive index change at the periphery of the central implant region **2123** located under the top anode electrode, and v) a refractive index change at the interface of the top DBR mirror that covers the sidewalls of the waveguide. The p-channel injector is located in a central well that is surrounded by the anode terminal. The well is defined by a mesa in the spacer layer **1713** disposed above the p-type modulation doped QW structure **1711**. P-type donor ions can be implanted through this mesas to form a p-type ion implant region **2125** that creates a self-aligned p-type contact to the p-type modulation doped quantum well structure **1711** of the active waveguide **2102**.

As shown in FIG. **21**D, the optical mode **2110**A that propagates through the zig-zag waveguide **2109**A is strongly confined within the zig-waveguide **2109**A by internal reflection at the reflective interfaces of the waveguide **2109**A. Specifically, cladding for guiding the optical mode **2110**A in the waveguide **2109**A can be provided by the top DBR mirror structure (not shown) and the bottom DBR mirror **1703**. Lateral confinement of the optical mode **2110**A in the waveguide **2109**A can be provided by i) a refractive index change at the sidewalls that define the outer boundary of the waveguide **2109**A, ii) a refractive index change at n-type ion implant region **2131**A that is disposed adjacent the top rib sidewalls of the waveguide **2109**A (not shown), and iii) a refractive index change at the interface of the top mirror that covers the sidewalls of the waveguide **2109**A. In the coupling region, the waveguide **2109**A includes a section that extends parallel to and is closely-spaced from a straight section of the microresonator waveguide **2102** by the gap region **2113**A. In this section of the waveguide **2109**A, lateral confinement of the optical mode **2110**A is provided by a refractive index change at the periphery of the implant region **2127**A under the metal of the coupling control electrode **2115**A as shown, and a refractive index change at the periphery of the implant region **2129**A in the coupling region (gap **2113**A) as evident from FIG. **18**D. In the coupling section of the microresonator waveguide **2102**, lateral confinement of the optical mode **2104** is further provided by a refractive index change at the periphery of the implant region **2129**A in the coupling region (gap G—**2113**A) as evident from FIG. **18**D. An n-type implant **2131**A is disposed under the control electrode **2117**A for contact to the n-type modulation-doped quantum well structure **1715** of the zig-zag waveguide **2109**A.

As shown in FIG. **21**D, the optical mode **2110**B that propagates through the zig-zag waveguide **2109**B is strongly confined within the zig-waveguide **2109**B by internal reflection at the reflective interfaces of the waveguide **2109**B. Specifically, cladding for guiding the optical mode **2110**B in the waveguide **2109**B can be provided by the top DBR mirror structure (not shown) and the bottom DBR mirror **1703**. Lateral confinement of the optical mode **2110**N in the waveguide **2109**B can be provided by i) a refractive index change at the sidewalls that define the outer boundary of the waveguide **2109**B, ii) a refractive index change at n-type ion implant region **2131**B that is disposed adjacent the top rib sidewalls of the waveguide **2109**A (not shown), and iii) a refractive index change at the interface of the top mirror that covers the sidewalls of the waveguide **2109**A. In the coupling region, the waveguide **2109**B includes a section that extends parallel to and is closely-spaced from a straight section of the microresonator waveguide **2102** by the gap region **2113**B. In this section of the waveguide **2109**B, lateral confinement of the optical mode **2110**B is provided by a refractive index change at the periphery of the implant region **2127**B under the metal of the coupling control electrode **2115**B as shown, and a refrac-

tive index change at the periphery of the implant region **2129**B in the coupling region (gap **2113**B) as evident from FIG. **18**D. In the coupling section of the microresonator waveguide **2102**, lateral confinement of the optical mode **2104** is further provided by a refractive index change at the periphery of the implant region **2129**B in the coupling region (gap G —**2113**B) as evident from FIG. **18**D. An n-type implant **2131**B is disposed under the control electrode **2117**B for contact to the n-type modulation-doped quantum well structure **1715** of the zig-zag waveguide **2109**B. The cathode terminal of the thyristor closed-path waveguide resonator **2101** is formed outside the resonator on a mesa located in the bottom n-type contact layer **1705** as shown.

For configuration as an optoelectronic oscillator, the thyristor closed-path waveguide resonator **2101** can be configured for digital optical-to-electrical conversion where the optical signal propagating in the waveguide **2102** generates photocurrent by absorption which adds electrons to the n-type modulation doped QW structure **1715** and holes to the p-type modulation doped QW structure **1711** such that the thyristor device switches ON and conducts current through the device between the anode terminal electrode and the cathode terminal electrode. Such optoelectronic operations provide the function of detection, current-to-voltage conversion (typically provided by a transimpedance amplifier), level shifting to obtain a ground reference and a decision circuit (typically realized by a comparator). Moreover, the thyristor closed-path waveguide resonator **2101** has an advantage that it will only absorb at the resonator frequency and thus can be adapted to support different wavelengths for wavelength division multiplexing applications. Moreover, the ON state current that flows between the anode terminal electrode and the cathode terminal electrode of the thyristor resonator is configured above the threshold for lasing I_{TH}, such that photon emission will occur within the device structure. In principle, the resonator produces light that propagates in both the clockwise and counterclockwise sense along the optical path of the resonant cavity waveguide **2102**. Moreover, the evanescent coupling across the gap region **2113**A between the resonant cavity waveguide **2102** and the zig-zag waveguide **1209**A operates on both clockwise and counterclockwise light propagation within the resonant cavity waveguide **2102**. Similarly, the evanescent coupling across the gap region **2113**B between the resonant cavity waveguide **2102** and the zig-zag waveguide **1209**B operates on both clockwise and counterclockwise light propagation within the resonant cavity waveguide **2102**.

In this configuration, the input optical pulse can be supplied to one end of the zig-zag waveguide **2019**A as shown in FIG. **21**A such that it propagates through the straight section of the zig-zag waveguide **2019**A adjacent the gap region **2113**A, where it couples into the waveguide **2102** by evanescent coupling for propagation within the waveguide **2102** as shown by the arrows of FIG. **21**B. The input pulse signal that propagates within the waveguide **2102** is then subject to digital optical-to-electrical conversion and pulse regeneration by the thyristor switch action as described herein.

A bragg-grating reflector **2121** is optically coupled to the zig-zag waveguide structure **210B9** opposite its output end as shown in FIG. **21**A. The bragg-grating reflector **212** is a linear active waveguide device formed as a light reflector that builds upon the multiple directions of light propagation in the resonant cavity waveguide **2102** of the resonator as well as the multiple directions of evanescent coupling provided between the zig-zag waveguide **2109**B and the resonant cavity waveguide **2102** of the resonator. The bragg-grating reflector **2121** has Bragg grating **2123** (such as a first-order or third-order Bragg grating) defined throughout the length of the active waveguide device. The Bragg grating **2123** can be defined by etching into the top layers (such as layers **1721**, **1719**, **1717** of layer structure of FIG. **17**) as best shown in FIGS. **21**E and **21**F. The Bragg grating **2123** operates to reflect any optical modes propagating in the zig-zag waveguide **2109**B in the direction of the reflector **2121** where the wavelength of such optical modes coincides with the Bragg frequency of the Bragg grating **2123**. All optical modes at other wavelengths will be passed through the tuning reflector **2121** or be absorbed. The Bragg grating **2123** can be configured such that the Bragg frequency of the Bragg grating **2123** closely matches the desired output wavelength for the resonator.

The pulse regeneration that results from the thyristor switching action of the resonator produces optical mode(s) that propagate clockwise within the resonant cavity waveguide **2102** of the resonant, which are coupled into the zig-zag waveguide **2109**B to produce optical mode(s) that propagate in the zig-zag waveguide **2109**B to the reflector **321**. The incident optical mode(s) at wavelengths that coincide with the Bragg frequency of the Bragg grating **2123** of the reflector **2121** are reflected back and propagate in the reverse direction within the zig-zag waveguide **2109**B where the mode is coupled into the resonator to produce optical mode(s) that propagates counter-clockwise in the resonant cavity waveguide **2102** of the resonator and generate more stimulated emission. This operation is repeated many times such that the wavelength of dominant optical mode that propagates in the resonant cavity waveguide **2102** of the resonator corresponds to the Bragg frequency of the Bragg grating **2123**. Such dominant optical mode propagating counter-clockwise in the resonant cavity waveguide **2102** of the resonator is coupled to the zig-zag waveguide **2109**B to produce the regenerated output optical pulse signal (which propagates in the direction away from the tuning reflector **2121** as shown in FIG. **21**A). In this manner, optical modes that coincide with the Bragg frequency of the Bragg grating **2123** of the reflector **2121** make double passes through the resonant cavity waveguide **2102** of the resonator for improved stimulated emission. This operation is repeated such that the wavelength of the dominant or primary optical mode that propagates in the resonant cavity waveguide **2102** of the resonator corresponds to the Bragg frequency of the Bragg grating **2123**. With this operation, the dominant or primary optical mode that propagates in the resonant cavity waveguide **2102** of the resonator is output from the zig-zag waveguide **2109**B, while optical modes that do not coincide with the Bragg frequency of the Bragg grating **2123** are removed from the output pulse signal by the operation of the reflector **2121**.

The Bragg grating **2123** functions as a narrow-band filter where the Bragg frequency of grating **2123** dictates the wavelength of the dominant or primary optical mode that propagates in the resonant cavity waveguide **2102** of the resonator. Such narrow-band filtering is useful for larger closed-loop resonators where the natural mode resonances are closely spaced from one another and thus do not provide a narrow wavelength band for the optical mode that propagates in the closed-loop resonator. It is also contemplated that the Bragg frequency of the Bragg grating **2123** can be electrically-controlled (or tuned) by controlled injection of charge that modifies the index of the region n2 of the Bragg grating 323 as described in U.S. patent application Ser. No. 14/222,841, filed on Mar. 24, 2014, commonly assigned to assignees of the present invention and herein incorporated by reference in its entirety.

It is also contemplated that the optical thyristor **2100** of FIGS. **21**A-**21**C can readily be configured as an optical thyristor for other circuit functions described herein. In one example, the optical thyristor **2100** of FIGS. **21**A-**21**C can be configured as part of the optical phase detector of FIGS. **3**A, **10**E, **10**H, and **10**I where the output optical signal that results from the switching action of the optical thyristor is output from output end of waveguide **2109**B. In another example, the optical thyristor **2100** of FIGS. **21**A-**21**C can be configured as part of the optical XOR gate of FIG. **8**A where the output optical signal C that results from the switching action of the optical thyristor is output from output end of waveguide **2109**B. In yet another example, the optical thyristor **2100** of FIGS. **21**A-**21**C can be configured as part of the optical flip-flops of FIGS. **13**A and **13**B where the input optical signal (D_A or D_B) are supplied to the one end of waveguide **2109**A (similar to the input optical pulse in FIG. **21**A), and the output optical signal (Q_A or Q_B) that results from the switching action of the optical thyristor is output from output end of waveguide **2109**B. In yet another example, the optical thyristor **2100** of FIGS. **21**A-**21**C can be configured as part of the optical-input AND gate of FIG. **14**A where the input optical signal Q_A is supplied to the one end of waveguide **2109**A (similar to the input optical pulse in FIG. **21**A), and the input optical signal Q_B is supplied to the other end of waveguide **2109**A. In still another example, the optical thyristor **2100** of FIGS. **21**A-**21**C can be configured as part of the optical charge pump of FIG. **15**A where the input optical signal (Q_A or Q_B) is supplied to the one end of waveguide **2109**A (similar to the input optical pulse in FIG. **21**A).

Polarization Diversity Systems

It is also common for PSK and QAM modulation schemes to be combined with polarization diversity where the modulated carrier wave signal employs light with orthogonal polarizations. In such systems, the coherent optical receiver designs as described herein can be replicated downstream of optical elements that split the received optical signal into multiple legs corresponding to the orthogonal polarizations and then processes each leg to isolate the optical signal of the corresponding polarization state for detection.

Wavelength Division Multiplexing (WDM) Systems

It is also common for PSK and QAM modulation schemes to be combined with wavelength division multiplexing where the modulated carrier wave signals can be defined by specific wavelengths of light. In such systems, the coherent optical receiver designs as described herein can be replicated downstream of optical elements that split the received optical signal into multiple legs corresponding to the specific light wavelengths and then processes each leg to isolate the optical signal of the corresponding wavelength for detection.

There have been described and illustrated herein several embodiments of a coherent optical receiver and parts thereof that can be used for a wide variety of communications and data processing applications. While particular embodiments of the invention have been described, it is not intended that the invention be limited thereto, as it is intended that the invention be as broad in scope as the art will allow and that the specification be read likewise. It will therefore be appreciated by those skilled in the art that yet other modifications could be made to the provided invention without deviating from its spirit and scope as claimed.

What is claimed is:

1. A charge pump circuit for an optical phase lock loop, the charge pump circuit comprising:

first and second optical thyristors, wherein said first optical thyristor is configured to receive a first digital optical signal input, and wherein said second optical thyristor is configured to receive a second digital optical signal input;

a first filter circuit operably coupled to said first optical thyristor;

first control circuitry operably coupled to terminals of said first optical thyristor and receiving a first digital electrical signal input corresponding to the second digital optical signal input;

a second filter circuit operably coupled to said second optical thyristor; and

second control circuitry operably coupled to terminals of said second optical thyristor and receiving a second digital electrical signal input corresponding to the first digital optical signal input;

wherein said first control circuitry is configured to control switching operation of said first optical thyristor that sources current to the first filter circuit in response to the levels of the first digital optical signal input and the first digital electrical signal input; and

wherein said second control circuitry is configured to control switching operation of said second optical thyristor that sinks current from the second filter circuit in response to the levels of the second digital optical signal input and the second digital electrical signal input.

2. A charge pump circuit according to claim **1**, wherein:

said first filter circuit performs integration of increases in voltage potential of a cathode terminal of said first optical thyristor over time; and

said second filter circuit performs integration of decreases in voltage potential of an anode terminal of said second optical thyristor over time.

3. A charge pump circuit according to claim **2**, wherein:

the result of the integration performed by said first filter circuit is an increasing voltage signal at the cathode terminal of said first optical thyristor whose change over time tracks the phase offset of the first digital optical signal input and the second digital optical input; and

the result of the integration performed by said second filter circuit is a decreasing voltage signal at the anode terminal of said second optical thyristor whose change over time tracks the phase offset of the second digital optical signal input and the first digital optical input.

4. A charge pump circuit according to claim **1**, wherein:

said first and second optical thyristors are each defined by an epitaxial layer structure that includes a bottom n-type cathode region, an intermediate p-type region formed above the bottom n-type region, an intermediate n-type region formed above the intermediate p-type region, and a top p-type anode region formed above the intermediate n-type region, wherein each optical thyristor includes an anode terminal electrically coupled to the top p-type anode region, an n-type injector terminal electrically coupled to the intermediate n-type region, a p-type injector terminal electrically coupled to the intermediate p-type region, and a cathode terminal electrically coupled to the n-type cathode region.

5. A charge pump circuit according to claim **4**, wherein:

said first control circuit includes a first field-effect transistor whose source-drain current path is electrically coupled between a positive voltage supply and the n-type injector terminal of said first optical thyristor, wherein the first digital electrical signal input corresponding to the second digital optical signal input is supplied to said first field-effect transistor in order to control switching operation of said first optical thyristor.

6. A charge pump circuit according to claim 5, wherein:
said first field-effect transistor comprises an n-channel HFET transistor having a gate terminal that receives the first digital electrical signal input corresponding to the second digital optical signal input.

7. A charge pump circuit according to claim 4, wherein:
said first control circuit includes a second field-effect transistor whose source-drain current path is electrically coupled between a negative or ground power supply and the p-type injector terminal of said first optical thyristor, wherein the first digital electrical signal input corresponding to the second digital optical signal input is supplied to said second field-effect transistor in order to control switching operation of said first optical thyristor.

8. A charge pump circuit according to claim 7, wherein:
said second field-effect transistor comprises an n-channel HFET transistor having a gate terminal that receives the first digital electrical signal input corresponding to the second digital optical signal input.

9. A charge pump circuit according to claim 4, wherein:
said second control circuit includes a third field-effect transistor whose source-drain current path is electrically coupled between a positive voltage supply and the n-type injector terminal of said second optical thyristor, wherein the second digital electrical signal input corresponding to the first digital optical signal input is supplied to said third field-effect transistor in order to control switching operation of the second optical thyristor.

10. A charge pump circuit according to claim 9, wherein:
said third field-effect transistor comprises an n-channel HFET transistor having a gate terminal that receives the second digital electrical signal input corresponding to the first digital optical signal input.

11. A charge pump circuit according to claim 4, wherein:
said first control circuit includes a fourth field-effect transistor whose source-drain current path is electrically coupled between a negative or ground power supply and the p-type injector terminal of said second optical thyristor, wherein the second digital electrical signal input corresponding to the first digital optical signal input is supplied to said fourth field-effect transistor in order to control switching operation of said second optical thyristor.

12. A charge pump circuit according to claim 11, wherein:
said fourth field-effect transistor comprises an n-channel HFET transistor having a gate terminal that receives the second digital electrical signal input corresponding to the first digital optical signal input.

13. A charge pump circuit according to claim 4, wherein:
the intermediate n-type and p-type regions of the epitaxial layer structure of the optical thyristor include an n-type modulation doped QW structure and a p-type modulation doped QW structure, respectively.

14. A charge pump circuit according to claim 13, wherein:
the first and second control circuits include at last one field effect transistor that includes an n-type QW channel formed by the n-type modulation doped QW structure of the epitaxial layer structure of the first and second optical thyristors and/or a p-type QW channel formed by the p-type modulation doped QW structure of the epitaxial layer structure of the first and second optical thyristors.

15. A charge pump circuit according to claim 4, wherein:
the epitaxial layer structure of the first and second optical thyristors comprises group III-V materials.

16. An optical phase lock loop comprising:
an optical clock source that generates an optical clock signal;
an optical phase detector that measures phase difference between a reference optical signal and the optical clock signal generated by the optical clock source;
a feedback circuit that is configured to generate first and second control signal inputs for supply to the optical clock source, wherein the feedback circuit comprises the charge pump circuit of claim 1.

17. An optical phase lock loop according to claim 16, wherein:
said optical clock source comprises another optical thyristor.

18. An optical phase lock loop according to claim 16, wherein:
said optical phase detector comprises an optical flip-flop realized by another optical thyristor.

19. An optical phase lock loop according to claim 16, wherein:
said optical phase detector comprises an optical AND gate realized by another optical thyristor.

20. An optical phase lock loop according to claim 16, wherein:
said optical phase detector comprises an AND gate realized by a thyristor.

21. An optical phase lock loop according to claim 16, which is configured to perform a clock recovery function.

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